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Integer factor based SVPWM approach for multilevel inverters with continuous and discontinuous switching sequences

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Abstract: The most extensively employed strategy to control the AC output of power electronic inverters is the pulse width modulation (PWM) strategy. Since three decades modulation hypothesis continues to draw considerable attention and interest of researchers with the aim to reduce harmonic distortion and increased output magnitude for a given switching frequency. Among different PWM techniques space vector modulation (SVM) is very popular. However, as the number of output levels of the multilevel inverter (MLI) increases, the implementation of SVM becomes more difficult, because as the number of levels increases the total number of switches in the inverter increases which will increase the total number of switching states, which will result in increased computational complexity and increased storage requirements of switching states and switching pulse durations. The present work aims at reducing the complexity of implementing the space vector pulse width modulation (SVPWM) technique in multilevel inverters by using a generalized integer factor approach (IFA). The performance of the IFA is tested on a three-level inverter-fed induction motor for conventional PWM (CPWM) which is a continuous SVPWM method employing a 0127 sequence and discontinuous PWM (DPWM) methods viz, DPWMMIN using 012 sequences and DPWMMAX using a 721 sequence.

Key words: integer factor approach, inverters, multilevel inverters, optimum switching sequence, space vector modulation, SVPWM

1. Introduction

The principle of any PWM method is to generate a train of switching pulses that synthesize the same fundamental volt-second average as that of target reference waveform within a switching cycle. But these switching pulses also generate harmonic components other than fundamental which are to be minimized. Also, the performance of various methods or algorithms to generate switching pulses has been the subject of considerable research work over the years [1–8]. The merits of a particular PWM implementation are based on the reduction in harmonics [5–15], RMS harmonic ripple for typical load like induction motor [2,7,8,12,15] and [16], first or second order filtered distortion performance factors [17]. Since the improvement is fractional with recent PWM methods a common approach to compare PWM variations is useful. In [2, 4–6, 12–15] and [18–24], the benefits of DPWM methods over CPWM are analysed in terms of harmonic loss and switching losses. The switching frequency for DPWM methods is chosen to be 1.5 kHz and for the CPWM method it is 1 kHz to facilitate the comparison of different PWM strategies at exactly the same phase leg switching frequencies per fundamental cycle [4–7, 11, 12, 23]. Researchers in the past have proposed various SVPWM implementation algorithms for MLIs. All these algorithms concentrate on developing simple ways to find the exact location of reference vector, sector and sub triangle identification, deriving nearest switching states, switching time calculation and switching sequence selection. This is to reduce the memory requirement of the controller by which implementation on low-cost controllers is feasible [8,10] and [23–26]. In [27] reverse mapping-based SVM is presented for an *n*-level inverter. The extension of this algorithm to the various DPWM methods is presented in [28]. In [29], decomposition-based SVM is presented, but extending this approach to the higher levels involves more decomposition stages. In the present work an integer factor-based SVPWM algorithm using generalized expressions applicable to any 'n' level inverter for both CPWM and DPWM methods is proposed by eliminating the need of referring to lookup tables.

2. Integer factor approach

In the SVM control method, the reference vector is moving through sub triangles in each sector in which the switching pulse duration of each switch has to vary to synthesize the required voltage level. One of the approaches to generate PWM pulses in SVM to control the inverter is presented in the block diagram shown in Fig. 1. In this approach, the required reference signals are generated by deriving the expressions to each switch. In the case of two-level inverters it can be done easily. But extending the two-level method to the MLI is not a simple task, as levels increases complexity increases. The present work is aimed to develop generalized equations using unique integer factors that satisfy the implementation of both continuous and different DPWM methods for any level inverter. The derived generalized equations are functions of switching times and levels of the inverter and in turn switching times are functions of integer factors. The required integer factors at every switching instant can be derived through simple algebraic expressions.

Hence the proposed IFA is more useful for the MLI, especially at a higher number of levels. This approach will involve identifying the reference vector location in terms of sector and sub-triangles, computation of switching times and deriving the generalized expressions to the reference

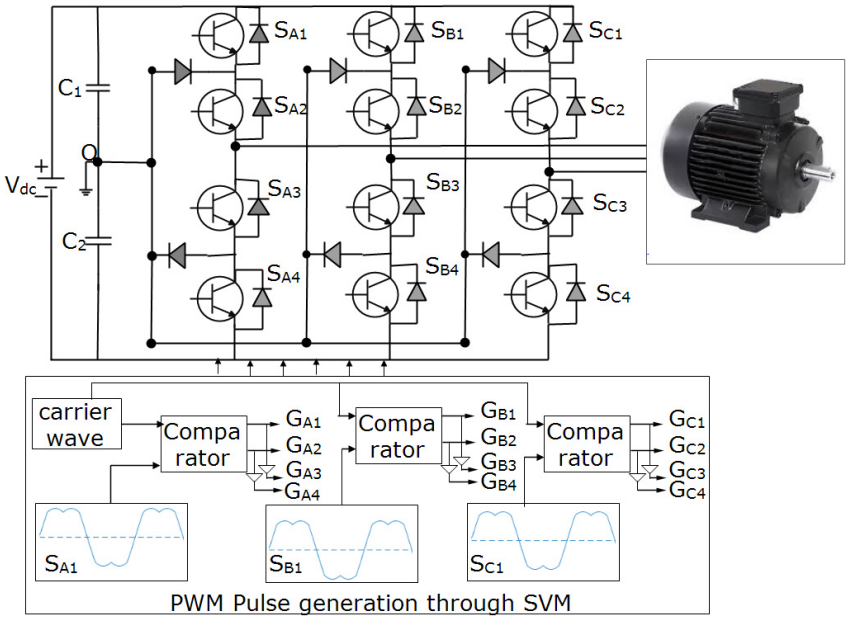
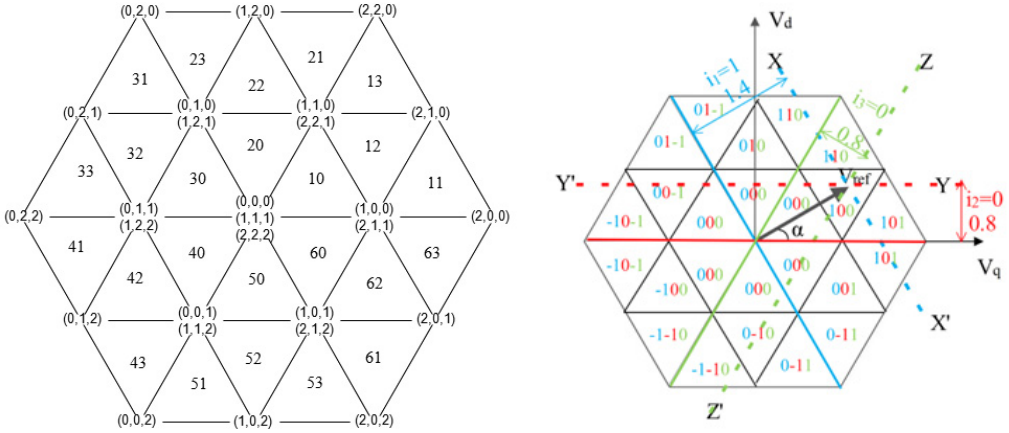


Fig. 1. Approach to generate PWM signals in the SVM control of the three level inverter

signal of each switch in the MLI. Let Fig. 2(a) show the state space plane of a three-level inverter with all the realizable switching states. It is a regular hexagon with six symmetrical sectors 'k' and each sector containing four sub-triangles designated by 'ij' where i refers to the sector number and j refers to the sub-triangle number of that sector. The sub-triangles are categorized as type-1 or type-2 depending on whether its apex is facing up or down. If the apex is facing upwards the triangle is called a type-1 triangle and if the apex is facing downwards then the triangle is type-2. For instance, in sector-1, out of four sub-triangles, three (10, 11, 13) are type-1 and one (12) is type-2.

2.1. Identifying the reference vector location in terms sub-triangle

The sub-triangle, in which the reference vector ($\boldsymbol{V}_{\mathbf{ref}}$) is located, is identified through the combination of integer factors of the corresponding sub-triangle. The space vector plane consists of three-line segments X-X^1, Y-Y^1', and Z-Z^1' which can slide back and forth relative to their reference axes. The reference axes are inclined at 120°, 0°, 60° with respect to the q-axis as shown in Fig. 2(b). At a given Modulation Index (MI) the tip of $\boldsymbol{V}_{\mathbf{ref}}$ that lies in a sub-triangle is identified by sliding the three-line segments so that it encloses the tip of $\boldsymbol{V}_{\mathbf{ref}}$. The three-line segments may take positive and/or negative real values depending on how much the axes slide from the corresponding reference axes to enclose the tip of $\boldsymbol{V}_{\mathbf{ref}}$. In this approach truncated values of shifted axes from their corresponding reference axes are designated by the integer factors i_1,i_2, and i_3. These integer factors will identify the sub-triangle that surrounds the tip of $\boldsymbol{V}_{\mathbf{ref}}$. Figure 2(b) shows the sub-triangles with a unique combination of i_1, i_2, and i_3. Integer factors are



(a) (b)

Fig. 2. State space diagram of three-level inverter: switching states and sub-triangles (a); integer factors in each sub-triangle (b)

derived using the set of equations given in (1)–(3), where V_d and V_q are the two-phase quantiles of the equivalent three-phase sinusoidal quantities. These are obtained from standard 3-phase to 2-phase conversion. The identification of the reference vector location in terms of sub-triangles is required to derive generalized expressions for the switching times.

$$i_1 = \text{integer}\left(V_d + \frac{V_q}{\sqrt{3}}\right), \tag{1}$$

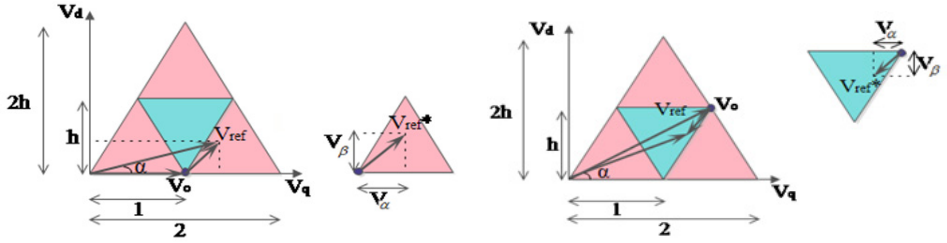
$$i_2 = \text{integer}\left(\frac{V_q}{\sqrt{3}}\right), \tag{2}$$

$$i_3 = \text{integer}\left(V_d - \frac{V_q}{\sqrt{3}}\right). \tag{3}$$

2.2. Determination of switching state times

After identifying the sub-triangle with help of unique combination of integer factors, the switching times are to be calculated. To calculate the switching times, the nearest switching states that lie at the corners of the sub-triangle need to be identified. For this $\boldsymbol{V}_{\mathbf{ref}}$ is shifted to a new origin and the new reference vector is here referred to as a shifted reference vector, $\boldsymbol{V}^*_{\mathbf{ref}}$. The new origin V_0 will be one of three vertices of the sub-triangle in which the tip of $\boldsymbol{V}_{\mathbf{ref}}$ is located. The d-q axes components of the $\boldsymbol{V}^*_{\mathbf{ref}}$ are designated as V_α, V_β, respectively, and these components for all the sectors are determined by using generalized expressions formulated in Table 1. For example, $\boldsymbol{V}_{\mathbf{ref}}$ in sector 1 and the transition from sub-triangle 11 to sub-triangle 13 followed by sub-triangle 12. Sub-triangle 11 is type-1, sub-triangle 12 is type-2 and sub-triangle 13 is again the type-1 sub-triangle. Let's suppose the $\boldsymbol{V}_{\mathbf{ref}}$ is in sub-triangle 11, i.e. the type-1 sub-triangle, the shifting of $\boldsymbol{V}_{\mathbf{ref}}$ is as shown in Fig. 3(a). Hence, the switching times to synthesize $\boldsymbol{V}_{\mathbf{ref}}$ will be the same as the switching times required to synthesize $\boldsymbol{V}^*_{\mathbf{ref}}$ located in the first sector of a two-level

inverter with V_0 as the middle. Similarly, shifting of $\boldsymbol{V}_{\mathbf{ref}}$ located in the type-2 sub-tringle is shown in Fig. 3(b). Hence, the switching times to synthesize $\boldsymbol{V}_{\mathbf{ref}}$ will be same as the switching times required to synthesize $\boldsymbol{V}^*_{\mathbf{ref}}$ located in the fourth sector of a two-level inverter with V_0 as the middle. The switching times for all sectors are tabulated in Table 2. In this approach, the factor $(-1)^{i1+i2+i3}$ discriminates the type of sub-triangle, based on which the switching times of the required states will be executed for optimum performance of the inverter.



(a) (b)

Fig. 3. Transit of $\boldsymbol{V}_{\mathbf{ref}}$ in Sector-1: shifted origin, coordinates of $\boldsymbol{V}^*_{\mathbf{ref}}$ in type-1 sub-triangle 11 (a); shifted origin, coordinates of $\boldsymbol{V}^*_{\mathbf{ref}}$ in type-2 sub-triangle 12 (b)

Table 1. Direct and quadrature axis components of shifted reference vector

k	Angle (α)	V_α	V_β
1	$0° \le \alpha \le 60°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 - 0.25) + 0.25$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) + 0.5h$
2	$60° \le \alpha \le 90°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 - 0.25) + 0.25$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) + 0.5h$
	$90° \le \alpha \le 120°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 + 0.75) - 0.75$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) + 0.5h$
3	$120° \le \alpha \le 180°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 + 0.75) - 0.75$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) + 0.5h$
4	$180° \le \alpha \le 240°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 + 0.25) - 0.25$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) - 0.5h$
5	$240° \le \alpha \le 270°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 + 0.25) - 0.25$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) - 0.5h$
	$270° \le \alpha \le 300°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 - 0.75) + 0.75$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) - 0.5h$
6	$300° \le \alpha \le 360°$	$(-1)^{i_1+i_2+i_3}(V_q + 0.5i_2 - i_1 - 0.75) + 0.75$	$(-1)^{i_1+i_2+i_3}(V_d - (i_2 * h) - 0.5h) - 0.5h$

Table 2. Active state switching times in different sectors

k	1	2	3	4	5	6
T_1	$T_s\left[V_\alpha - \frac{V_\beta}{\sqrt{3}}\right]$	$T_s\left[-V_\alpha + \frac{V_\beta}{\sqrt{3}}\right]$	$T_s\left[\frac{V_\beta}{h}\right]$	$-T_s\left[V_\alpha - \frac{V_\beta}{\sqrt{3}}\right]$	$-T_s\left[-V_\alpha + \frac{V_\beta}{\sqrt{3}}\right]$	$-T_s\left[\frac{V_\beta}{h}\right]$
T_2	$T_s\left[\frac{V_\beta}{h}\right]$	$T_s\left[V_\alpha + \frac{V_\beta}{\sqrt{3}}\right]$	$T_s\left[-V_\alpha - \frac{V_\beta}{\sqrt{3}}\right]$	$T_s\left[\frac{V_\beta}{h}\right]$	$-T_s\left[V_\alpha + \frac{V_\beta}{\sqrt{3}}\right]$	$-T_s\left[-V_\alpha - \frac{V_\beta}{\sqrt{3}}\right]$

2.3. Generalized expressions for the switching pulse duration

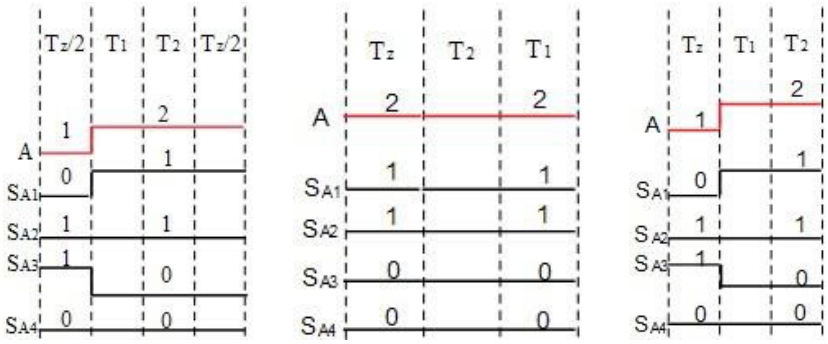
The major difficulty in the SVPWM approach is to synthesize $\boldsymbol{V}_{\mathbf{ref}}$ through various switching pulses. Hence, the proposed scheme develops a set of generalized equations to each switch of the MLI using the IFA in the CPWM and DPWM methods. As integer factors are unique for a sub-triangle in a sector, the equations which are a function of integer factors and n will automatically adapt to synthesize the reference waves of all switches. Hence, it eliminates the need of lookup tables. Figure 4 shows the timing diagram of phase A in sector 1 for the 0127 sequence of a three-level inverter. Here T_1, T_2, T_z are the switching times which are calculated in the previous section. States 2, 1, 0 represent the switch positions (on or off) to synthesize three levels from the inverter. State 2 indicates that the top 2 switches of a phase are on, 1 means the middle two switches are on and 0 means the bottom two switches are on. From the timing diagram the expression for the modulating waveforms is derived. For switches of phase A in sub-triangle 11 the equations of the modulating waveforms are given by Eqs. (4)–(7).

$$S_{A1} = T_1 + T_2 + \frac{T_Z}{2}, \tag{4}$$

$$S_{A2} = T_1 + T_2 + T_Z, \tag{5}$$

$$S_{A3} = \frac{T_Z}{2}, \tag{6}$$

$$S_{A4} = 0. \tag{7}$$



(a) (b) (c)

Fig. 4. Timing diagram of phase A: 0127 sequence (a); 721 sequence (b); 012 sequence (c)

The expressions for the remaining phases are also obtained from the timing diagrams in a similar manner. The timing diagram shown above is for sub triangle 11 which is the type-1 triangle. Similarly, for the type-2 triangle the switching expressions are to be obtained from the timing diagram.

The switching expressions for type-1 and type-2 are almost similar but differ by factors U and V which take either 0 or 1. Hence, the generalized expressions are to be developed as functions of integer factors, U, V which can adapt itself with the type of the sub-triangle and suits to any level of the inverter. From Fig. 2(b) it can be observed that the sub-triangles corresponding to the

three-level inverter, in sector 1, will have a common integer factor, i_1. Similarly, each sector will have a common integer factor. Table 3 shows the common integer factor for all the six sectors.

Table 3. Common integer factor for each sector

Sector	**1**	**2**	**3**	**4**	**5**	**6**
Common integer factor	i_1	i_2	i_3	i_1	i_2	i_3

The generalized expressions for each sector are expressed in terms of the common factor. The expressions for phase A, for type-1 and type-2 sub-triangles in sector 1, are given by Eqs. (8) and (9), respectively. Here, S_{Ap} is the switching pulse duration expression for the phase A switches in a particular sampling period T_s, where p indicates the switch number which varies from 1 to $(n-1)$ and n is the level of the inverter. Equations (8) and (9) are combined to get one generalized expression of (10) and (11). The sum of i_1, i_2 and i_3 is even for the type-1 triangle and odd for the type-2 triangle. So, the value of $(-1)^{i_1+i_2+i_3}$ equals 1 for the type-1 triangle and 0 for the type-2 triangle, and so, U becomes 0 and V becomes 1 for the type-1 triangle and vice versa for the type-2 triangle.

$$S_{Ap} = p\left[\frac{T_z}{n-i_1} + \frac{T_1}{n-i_1-1} + \frac{T_2}{n-i_1-1}\right], \tag{8}$$

$$S_{Ap} = p\left[\frac{T_z}{n-i_1-1} + \frac{T_1}{n-i_1} + \frac{T_2}{n-i_1}\right], \tag{9}$$

$$U = \frac{1}{2}\left[1-(-1)^{i_1+i_2+i_3}\right], \tag{10}$$

$$V = \frac{1}{2}\left[1+(-1)^{i_1+i_2+i_3}\right]. \tag{11}$$

Hence, the generalized switching pulse duration expression for the reference vector present in sector 1 of phase A changes to (19), which is valid for both types of sub-triangles. For the three-level inverter p takes 1 and 2. The switching pulses for the remaining switches 3 and 4 will be obtained by inverting the pulses of 1 and 2. So, Eq. (12) will be the switching pulse duration expression for phase A in sector 1. Similarly, the switching pulse duration expressions for phases B and C are derived and are given by Eqs. (13) and (14).

$$S_{Ap} = p\left[\frac{T_z}{n-i_{1\_}U} + \frac{T_1+T_2}{n-i_1-V}\right], \tag{12}$$

$$S_{Bp} = (p-i_3-L)\left[\frac{T_z}{n-i_{1\_}U} + \frac{T_2}{n-i_1-V}\right] + (p-i_3-H)\left[\frac{T_1}{n-i_1-V}\right], \tag{13}$$

$$S_{Cp} = (p-i_3-L)\left[\frac{T_z}{n-i_{1\_}U}\right] + (p-i_3-H)\left[\frac{T_1+T_2}{n-i_1-V}\right]. \tag{14}$$

Equations (12) to (14) are the switching pulse expressions for the three phases that are valid for all sub-triangles of sector 1. It is observed that the three expressions have a common integer factor, i_1. Similarly, the switching pulse duration expressions for all the remaining sectors can be derived and are tabulated in Table 4.

Table 4. Switching pulse duration expressions of all sectors for 0127 sequence

k	**Phase A**	**Phase B**	**Phase C**
1	$P\left[\frac{T_z}{n-i_{1-}U}+\frac{T_1+T_2}{n-i_1-V}\right]$	$(p-i_3-U)\left[\frac{T_z}{n-i_1-U}+\frac{T_2}{n-i_1-V}\right]+(p-i_3-V)\left[\frac{T_1}{n-i_1-V}\right]$	$(p-i_3-U)\left[\frac{T_z}{n-i_1-U}\right]+(p-i_3-V)\left[\frac{T_1+T_2}{n-i_1-V}\right]$
2	$(p-i_3-U)\left[\frac{T_z}{n-i_2-U}+\frac{T_2}{n-i_2-V}\right]+(p-i_3-V)\left[\frac{T_1}{n-i_2-V}\right]$	$p\left[\frac{T_z}{n-i_2-U}+\frac{T_1+T_2}{n-i_2-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_2-U}\right]+(p-i_2-V)\left[\frac{T_1+T_2}{n-i_2-V}\right]$
3	$(p-i_3-U)\left[\frac{T_z}{n-i_3-U}\right]+(p-i_3-V)\left[\frac{T_1+T_2}{n-i_3-H}\right]$	$p\left[\frac{T_z}{n-i_3-U}+\frac{T_1+T_2}{n-i_3-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_3-U}+\frac{T_2}{n-i_3-V}\right]+(p-i_2-V)\left[\frac{T_1}{n-i_3-V}\right]$
4	$(p-i_1-U)\left[\frac{T_z}{n-i_1-U}\right]+(p-i_{21}-V)\left[\frac{T_1+T_2}{n-i_1-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_1-U}+\frac{T_2}{n-i_1-V}\right]+(p-i_2-V)\left[\frac{T_1}{n-i_1-V}\right]$	$p\left[\frac{T_z}{n-i_1-U}+\frac{T_1+T_2}{n-i_1-V}\right]$
5	$(p-i_1-U)\left[\frac{T_z}{n-i_2-U}+\frac{T_2}{n-i_2-V}\right]+(p-i_1-V)\left[\frac{T_1}{n-i_2-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_2-U}\right]+(p-i_{22}-V)\left[\frac{T_1+T_2}{n-i_2-V}\right]$	$p\left[\frac{T_z}{n-i_2-U}+\frac{T_1+T_2}{n-i_2-V}\right]$
6	$p\left[\frac{T_z}{n-i_3-U}+\frac{T_1+T_2}{n-i_3-V}\right]$	$(p-i_3-U)\left[\frac{T_z}{n-i_3-U}\right]+(p-i_{23}-V)\left[\frac{T_1+T_2}{n-i_3-V}\right]$	$(p-i_1-U)\left[\frac{T_z}{n-i_3-U}+\frac{T_2}{n-i_3-V}\right]+(p-i_1-V)\left[\frac{T_1}{n-i_3-V}\right]$

3. Extension of the proposed IFA to discontinuous PWM methods

Further, to exploit the advantages of DPWM methods the proposed approach is extended to various DPWM methods using either 012 and/or 721 witching sequences [4–7, 11, 16]. The switching pulse duration expressions for sequences 721 and 012 in the different sectors can be derived based on the timing diagrams shown in Fig. 4(b) and Fig. 4(c) for sub-triangle 11. Expressions are tabulated in Table 5.

Table 5. Switching pulse duration expressions of all sectors for 721 sequence

k	**Phase A**	**Phase B**	**Phase C**
1	$p\left[\frac{T_z}{n-i_1-V}+\frac{T_1+T_2}{n-i_1-V}\right]$	$(p-i_3-U)\left[\frac{T_z}{n-i_1-V}+\frac{T_2}{n-i_1-V}\right]+(p-i_3-V)\left[\frac{T_1}{n-i_1-V}\right]$	$(p-i_3-U)\left[\frac{T_z}{n-i_1-V}\right]+(p-i_3-V)\left[\frac{T_1+T_2}{n-i_1-V}\right]$
2	$(p-i_3-U)\left[\frac{T_z}{n-i_2-V}+\frac{T_2}{n-i_2-V}\right]+(p-i_3-V)\left[\frac{T_1}{n-i_2-V}\right]$	$P\left[\frac{T_z}{n-i_2-V}+\frac{T_1+T_2}{n-i_2-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_2-V}\right]+(p-i_2-V)\left[\frac{T_1+T_2}{n-i_2-V}\right]$
3	$(p-i_3-U)\left[\frac{T_z}{n-i_3-V}\right]+(p-i_3-V)\left[\frac{T_1+T_2}{n-i_3-V}\right]$	$P\left[\frac{T_z}{n-i_3-V}+\frac{T_1+T_2}{n-i_3-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_3-V}+\frac{T_2}{n-i_3-V}\right]+(p-i_2-V)\left[\frac{T_1}{n-i_3-V}\right]$
4	$(p-i_1-U)\left[\frac{T_z}{n-i_1-V}\right]+(p-i_{21}-V)\left[\frac{T_1+T_2}{n-i_1-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_1-V}+\frac{T_2}{n-i_1-V}\right]+(p-i_2-V)\left[\frac{T_1}{n-i_1-V}\right]$	$p\left[\frac{T_z}{n-i_1-V}+\frac{T_1+T_2}{n-i_1-V}\right]$
5	$(p-i_1-U)\left[\frac{T_z}{n-i_2-V}+\frac{T_2}{n-i_2-V}\right]+(p-i_1-V)\left[\frac{T_1}{n-i_2-V}\right]$	$(p-i_2-U)\left[\frac{T_z}{n-i_2-V}\right]+(p-i_{22}-V)\left[\frac{T_1+T_2}{n-i_2-V}\right]$	$p\left[\frac{T_z}{n-i_2-V}+\frac{T_1+T_2}{n-i_2-V}\right]$

Table 5 [cont.]

k	Phase A	Phase B	Phase C
6	$p\left[\frac{T_z}{n-i_{3-}V}+\frac{T_1+T_2}{n-i_3-V}\right]$	$(p-i_3-U)\left[\frac{T_z}{n-i_{3-}V}\right]+$ $(p-i_{23}-V)\left[\frac{T_1+T_2}{n-i_3-V}\right]$	$(p-i_1-U)\left[\frac{T_z}{n-i_3-V}+\frac{T_2}{n-i_3-V}\right]+$ $(p-i_1-V)\left[\frac{T_1}{n-i_3-V}\right]$

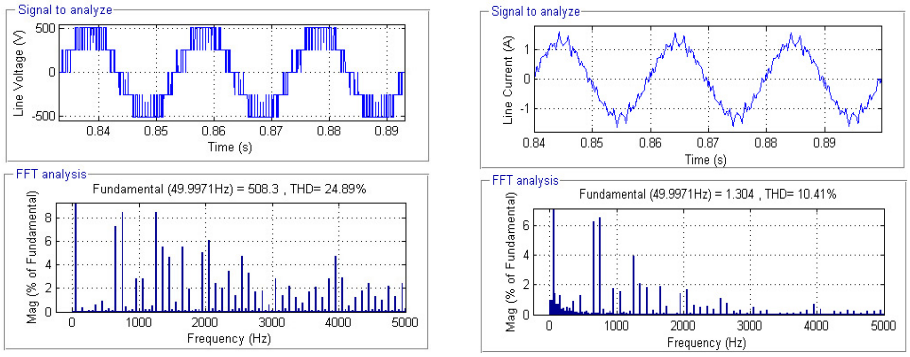
After determining the switching pulse durations for each switch, the actual gating pulses $G_{S_{A1}}$, $G_{S_{A2}}$, $G_{S_{B1}}$, $G_{S_{B2}}$, $G_{S_{C1}}$, $G_{S_{C2}}$ of different switches in the MLI are obtained by comparing the reference waveform of each switch with the carrier wave as represented in Fig. 1. The modulating waveform of switches S_{A1}, S_{B1}, S_{C1} will range from $-T_s$ to T_s and the modulating waveform of switches S_{A2}, S_{B2}, S_{C2} will range from 0 to $2T_s$. The carrier wave will be ranged from 0 to T_s. So, for the modulating waveforms of switches S_{A1}, S_{B1}, S_{C1}, the upper part, i.e., 0 to T_s, will be compared in a comparator with the carrier wave for generating the gating pulses, similarly, for the switches S_{A2}, S_{B2}, S_{C2}, the lower part, i.e., 0 to T_s, will be compared with the carrier wave to generate the gating pulses.

In Table 5, it can be observed that the expression for both switches of phase A in sector 1 and sector 6 will become T_s. This is obvious since phase A will be clamped onto the positive dc rail for 120° . Similarly, phases B and C will be clamped onto the positive dc rail, each for 120° in sectors 2, 3 and 4, 5, respectively. Similar explanation is valid for the 012 sequence except that each phase will be clamped onto the negative dc rail. Numerical analysis was done for all the considered PWM methods using the derived expressions. Clamping of phase A for various PWM methods can be observed by considering two switching instants of the reference vector, one at 10° and the other at 130° (in sector 1 and sector 3).

4. Simulation and experimental results

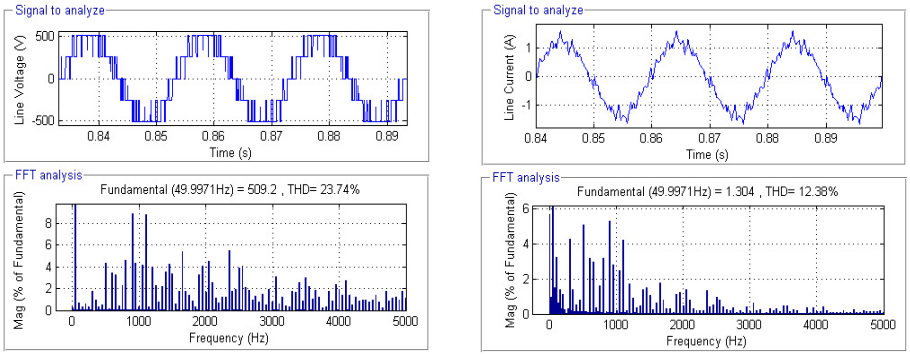
The performance of the proposed integer factor-based SVPWM algorithm is verified through MATLAB Simulink, using a three-level inverter-fed induction motor at no load without any filters and the same is validated experimentally. The parameters of the induction motor considered are 3−Φ, 0.75 kW, 415 V, 1.8 A, and 1415 rpm. The induction motor is controlled through the volts/Hz method. To show that, the proposed IFA is working for various switching sequences, the simulation has been done for sequences of 0127, 721 and 012. The simulation results of the inverter output line voltage and motor line current waveforms are presented in Fig. 5 to Fig. 7 for different space vector switching sequences at a modulation of 0.866. The experimental investigation is carried using a dSPACE1104 RTI control desk and results are presented in Fig. 8.

Figure 5(a) and Fig. 5(b) show motor line voltage and line current waveforms with THD for a switching sequence of 0127. Figure 6(a) and Fig. 6(b) show motor line voltage and line current waveforms with THD for a switching sequence of 721. Figure 7(a) and Fig. 7(b) show motor



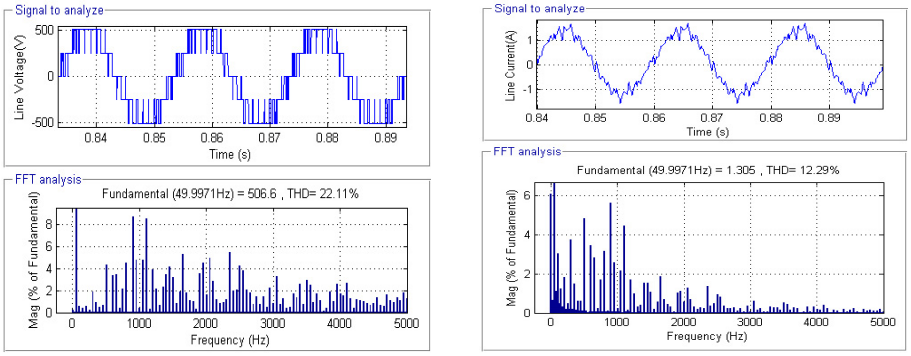
(a) (b)

Fig. 5. Simulation results at MI of 0.866 with 0127 sequence: line voltage waveform with THD (a); line current waveform with THD (b)



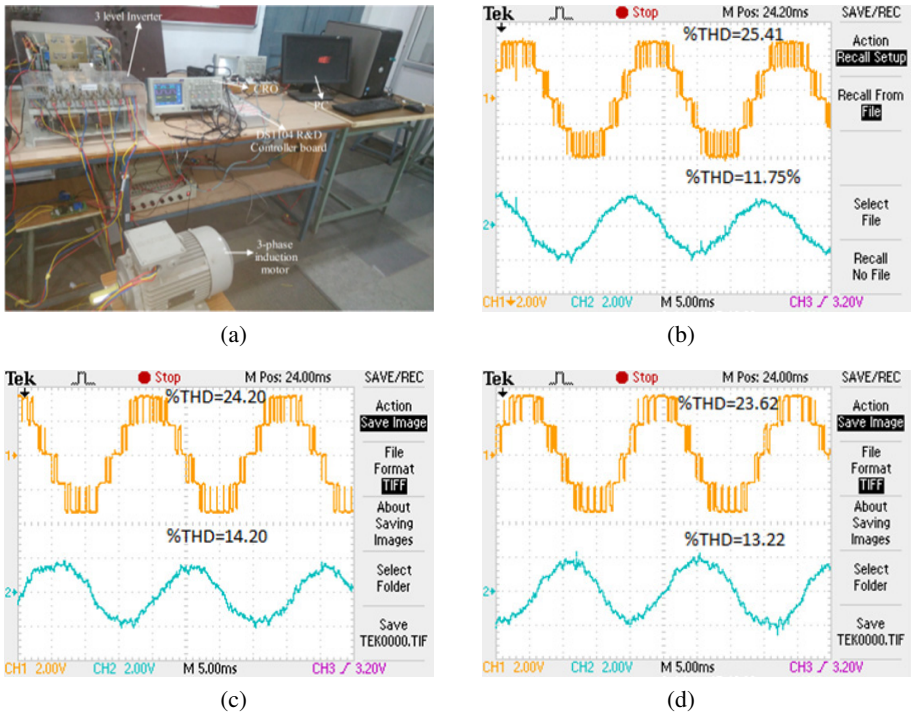
(a) (b)

Fig. 6. Simulation results at MI of 0.866 with 721 sequence: line voltage waveform with THD (a); line current waveform with THD (b)



(a) (b)

Fig. 7. Simulation results at MI of 0.866 with 012 sequence: line voltage waveform with THD (a); line current waveform with THD (b)



(a) (b)

(c) (d)

Fig. 8. Three-level inverters fed induction motor: hardware setup (a); line voltage and current at MI of 0.866 for 0127 sequence (b); line voltage and current at MI of 0.866 for 721 sequence (c); line voltage and current at MI of 0.866 for 012 sequence (d)

line voltage and line current waveforms with THD for a switching sequence of 012. Figure 8(a) shows the hardware setup of a three-level inverter-fed induction motor. Figure 8(b) shows the experimental results of inverter output line voltage and induction motor current waveforms at a modulation index of 0.866 for the 0127-sequence. Similarly, Fig. 8(c) and Fig. 8(d) show the experimental result of inverter output voltage and induction motor current waveforms at a modulation index of 0.866 for the 721 sequence and 012 sequence. By observing simulation and experimental results one can conclude that they are similar.

5. Conclusions

The SVPWM implementation through computation of switching pulse durations to continuous and discontinuous sequences for MLIs is implemented for a three-level inverter. Simplification is achieved through IFA where in sectors, sub-triangle identification to estimate the location of the reference vector is made. This algorithm is generalized for any levels and so, the number of steps required for implementation of any PWM method does not alter. The implementation of the scheme for the CPWM method is validated through the hardware implementation on a three-level

inverter-fed induction motor drive using a DS1104 R&D controller board. The SVPWM logic developed can further be extended to any MLI topology. Further, the scheme can be extended to any DPWM methods like DPWM MIN, DPWM MAX, DPWM 0, DPWM 1, DPWM 2, and DPWM 3.

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