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SEMICONDUCTOR CONTACT LAYER CHARACTERIZATION IN A CONTEXT OF HALL EFFECT MEASUREMENTS

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Abstract

A revision of the standard approach to characterization of thin-semiconductor-layer Hall samples has been proposed. Our results show that simple checking of I(V) curve linearity at room temperature might be insufficient for correct determination of bias conditions of a sample before measurements of Hall effect. It is caused by the nonlinear behaviour of electrical contact layers, which should be treated together with the tested layer *a priori* as a metal-semiconductor-metal (MSM) structure. Our approach was examined with a Be-doped p-type InAs epitaxial layer, with four gold contacts. Despite using full high-quality photolithography a significant asymmetry in maximum differential resistance (R_d) values and positions relative to zero voltage (or current) value was observed for different contacts. This suggests that such characterization should be performed before each high-precision magneto-transport measurement in order to optimize the bias conditions.

Keywords: metal contact, contact layer, contact resistance, Hall effect, resistivity, van der Pauw method, MSM structure, semiconductors' characterization.

1. Introduction

Nearly 140 years have passed since the discovery of the Hall effect in 1879 [1]. Until today hundreds of applications of this effect have been used, especially in the sensor technique, for measuring such parameters as: rotating speed, fluid flow, current or pressure [2]. However, despite a broad scope of applications, probably still the most frequent area of using this effect is characterization of material properties. A special significance in this area is reserved for measurements of a thin film's electronic properties [3], including anisotropic material systems [4]. Nowadays, more and more precise techniques are available. The multicarrier analysis, in which conductivity channels with less than 1% of total contribution are measurable, becomes a standard [5, 6]. In this situation more and more technological and measurement details begin to play an important role in extending the range of measurable data acquisition.

In this paper we would like to draw attention of the reader on selected aspects of the metallization-contact-layer-fields' quality problem. Generally, the reports containing information about

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manufacturing, formation and characterization of such a layer in the Hall effect measurements, have been frequently published in the literature [7], especially in a context of low-dimensional structures like: nanowires [8], graphene [9, 10], or quantum wells [11]. In most cases, regardless of the material being tested, the ohmic type contact is expected, even in the case of advanced numerical simulation [12]. Usually, the aim of research is not the contact layer itself, thus only a simple test on linearity of a current-voltage characteristic is being performed. As a standard, this is made only at room temperature. This simplified procedure can lead to the appearance of factors disturbing the resistivity and Hall effect measurement results, especially to their temperature dependence. The origin of this perturbation can be explained by forming the Schottky barriers between the metallization-contact layer and the tested semiconductor. Thus, a more realistic view on the high-precision measurements of Hall effect should *a priori* assume that the *device under test* (DUT) is composed of Schottky barriers in head-to-head (Fig. 1a), or back-to-back (Fig. 1b) configurations in series with a resistor between them [13, 14]. Therefore, it can be considered the same as *metal-semiconductor-metal* (MSM) electronic devices.

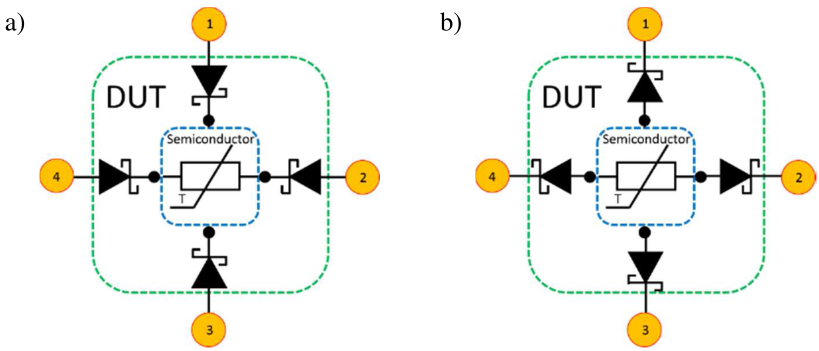

Fig. 1. A realistic equivalent circuit of a Hall sample in the 4-contact van der Pauw configuration for two different cases: Schottky barriers are connected head-to-head in series with a resistor inside (Fig. 1a), or similarly back-to-back in series (Fig. 1b).

As a consequence, non-linear regions in current-voltage I(V) or voltage-current V(I) characteristics, according to the thermionic emission theory, should be expected.

2. Experiment

2.1. Materials

In the experiment a Be-doped p-type InAs epitaxial layer was chosen. The layer was grown on a 2″ diameter and 0.4 mm thick GaAs semi-insulating substrate, using the RIBER Compact 21-DZ solid source *molecular beam epitaxy* (MBE) system. The system was equipped with standard and valved cracker effusion cells for Ga, In, Be and As, respectively. The p-InAs growth was preceded by a 0.25 μm thick GaAs layer to improve the substrate surface morphology after the degassing process. All necessary parameters of the performed growth are collected in Table 1.

Table 1. Growth conditions of a p-type InAs layer.

Layers	Thickness [µm]	V/III flux ratio	Temperature of cell [°C]							Growth rate [µm/h]	Temp. of manipulator [°C]
			Ga		As		In		Be		
			Tip	Base	Cracker	Reservoir	Tip	Base			
GaAs	0.25	3.2	1000	897	900	372	–	–	–	1.00	655
InAs	2.00	4.5	–	–	900	372	905	734	830	0.54	400

2.2. Sample preparation

The preparation of a Hall effect sample was performed by an advanced semiconductor processing treatment. The standard photolithography has been used to define contact areas and a circular measurement field using a positive photoresist AZ 4533 and NaOH water solution developer. The electrolytic anodization has been carried out to make the gold contacts. Electrolytic deposition of gold has been accomplished using an Au anode in the 1.2% (w/w) $KAu(CN)_2$ water solution [15, 16]. Finally, wet etching of the remaining area of the sample to the GaAs substrate has been carried out using the water solution of orthophosphoric acid, citric acid, hydrogen peroxide and hydrochloric acid [17]. Each contact area has been bonded with a 20 µm thick gold wire using a wire bonder machine. The sample has been attached to the sample holder by Apiezon grease and gold wires have been fixed to the sample holder pins using a silver powder suspension of thermoplastic poly-acrylic resin. The final shape and contacts' configuration of the sample is shown in Fig. 2.

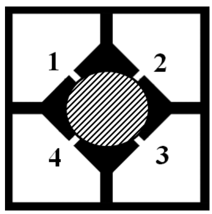

Fig. 2. A DUT with a 2 mm diameter circular measurement area and four large contacts with 200 × 300 µm contact paths.

2.3. Measurement

The samples attached to holders have been inserted into the Cryogenic Ltd CFMS cryostat system. The samples were placed directly in the circulating helium gas as a coolant agent. Temperature values (T_i) were monitored by two Cernox™ thermometers connected with a Lakeshore 218 Temperature Monitor. The first one was placed at the bottom of the cryostat and the second one 5 mm away from the sample, at the bottom side of the sample holder. The temperature stabilization was maintained by two heaters connected by PID loops into a multichannel Lakeshore 350 controller. All data have been gathered in the linearly-changed-temperature mode at a 0.5 K/min ramp rate across the whole temperature range: from 10 to 300 K.

All electrical measurements have been performed in the 2-contact mode, using an Agilent B2902A two-channel programmable multi-meter. The sample has been biased by a voltage source with simultaneous measurement of current. Examples of I(V) characteristics have been recorded alternatively for two different configurations of contact pairs (1–2, 3–4, see Fig. 2) on separated channels. Such a measurement mode enabled to acquire 15 I(V) characteristics (101 V-points) in a range: T_i −0.5 K < T_i < T_i + 0.5 K, for each channel and to obtain an averaged single I(V, T_i) result.

3. Results and discussion

A Hall element can be supplied either in the current or voltage mode [18]. For this reason an example of I(V) characteristics versus temperature has been taken into consideration and presented in Fig. 3.

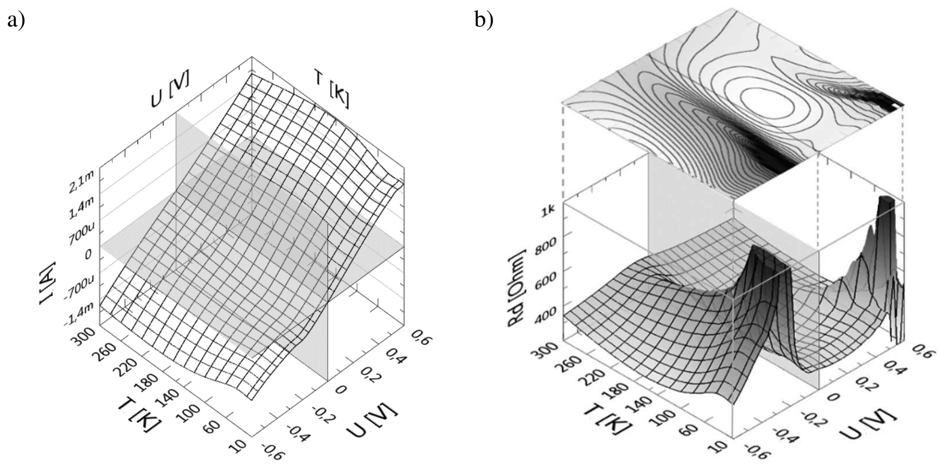

Fig. 3. An example of electrical characteristics versus temperature of a 4-contact Hall element. Here, for 1–2 contacts' configuration. a) I(V, T), b) R_d(V, T) with contour chart projection.

In the ideal case, without a Schottky contact influence, the I(V, T) surface should be linear in the I(V) direction. The same situation could be expected for the V(I, T) surface. However, the obtained results revealed a deviation from this regularity, especially below 200 K. The shadowed planes crossing the surfaces at $U = 0$ V have been added for better indication of the positive and negative sides of biases (Fig. 3a).

Differential resistance surfaces R_d(V, T), shown in Fig. 3b, have been calculated as follows: $R_d = (\Delta I/\Delta U)^{-1}$. Two strong local R_d extrema are visible in the figure, which can be easily determined from the contour chart plane at the top of Fig. 3b. These extrema occur on the positive as well as negative bias sides as a result of two Schottky junctions' contribution in the contact 1–2 (see Fig. 1a). Moreover, the strong asymmetry in maximum R_d values and positions relative to zero voltage value is observed. It is a consequence of different voltage drops on each contacts. The influence of these contacts on total resistance decreases when temperature increases and is negligible close to the room temperature. The similar characterization should be done for all contact configurations (*i.e.*: 2–3, 3–4, 4–1) before the target measurement of the resistivity and Hall constant. Almost identical surface could be observed in the case of R_d(I, T) – not presented here. It might be recalculated directly from R_d(V, T) using a suitable approximation method, like the spline approximation.

Thanks to the presented approach, relatively easy determination of the dependence of R_d *minima* on temperature is possible. In these conditions the total resistance value should be closest to the resistance of the examined semiconductor epitaxial layer. Precise knowledge of the I(V, T) or V(I, T) trends enables to select proper bias conditions during the resistivity and Hall effect measurement using the Van der Pauw method. It may have the crucial impact on obtaining a higher resolution capability using such techniques as *e.g.* analysis of mobility spectra.

4. Conclusions

In summary, we have proposed a revision of the standard approach to characterization of thin semiconductor-layer Hall samples. We assumed that an MSM structure always reveals its specific behaviour in changing voltage (current) supply and temperature associated with the appearance of Schottky barriers. Our results show that simple checking of I(V) linearity at room temperature might be insufficient for correct determination of the supply conditions of a sample during measurements of Hall effect. The method proposed in this work has been performed using a Be-doped p-type InAs epitaxial layer, processed to obtain a Hall effect sample with four gold contacts. Despite using full high-quality photolithography a noticeable asymmetry in maximum R_d values and positions relative to zero voltage (or current) value was observed for different contacts. This suggests that such characterization should be performed before each measurement of Hall effect in order to optimize the power conditions.

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