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Performance Comparison of Stacked Dual-Metal Gate Engineered Cylindrical Surrounding Double-Gate MOSFET

Abha Dargar and Viranjay M. Srivastava

***Abstract*—In this research work, a Cylindrical Surrounding Double-Gate (CSDG) MOSFET design in a stacked-Dual Metal Gate (DMG) architecture has been proposed to incorporate the ability of gate metal variation in channel field formation. Further, the internal gate's threshold voltage (V_{TH1}) could be reduced compared to the external gate (V_{TH2}) by arranging the gate metal work-function in Double Gate devices. Therefore, a device design of CSDG MOSFET has been realized to instigate the effect of Dual Metal Gate (DMG) stack architecture in the CSDG device. The comparison of device simulation shown optimized electric field and surface potential profile. The gradual decrease of metal work function towards the drain also improves the Drain Induced Barrier Lowering (DIBL) and subthreshold characteristics. The physics-based analysis of gate stack CSDG MOSFET that operates in saturation involving the analogy of cylindrical dual metal gates has been considered to evaluate the performance improvements. The insights obtained from the results using the gate-stack dual metal structure of CSDG are quite promising, which can serve as a guide to further reduce the threshold voltage roll-off, suppress the Hot Carrier Effects (HCEs) and Short Channel Effects (SCEs).**

***Keywords*—short-channel effects, metal-oxide-semiconductor transistor, cylindrical surrounding double-gate, dual-material gate, microelectronics, nanotechnology.**

I. Introduction

THE most significant invention is to miniaturize the component and device in the present era of microelectronics development as the increase of system complexity and speed has been a continuous challenge thus far. The semiconductor technology has a significant impact on the Very Large Scale Integrated (VLSI) device's consistent growth. The transistor size, which has reduced down towards nanometre miniaturization in the past three decades due to technical developments, has led to the craving of several improvements in device and performance parameters, including a decrease in operating voltage, increasing speed, and higher packaging densities [1]. The Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) transistor is a vital device in digital circuits that is the most promising element of an Integrated Circuit (IC) as a switching component to produce digital logic representation.

The MOSFET device can be made in a manner in which the semiconductor layer is over a buried-oxide (BOX) known as Silicon on Insulator (SOI) design. When the channel positioned in the middle of the BOX and gate insulator is precisely thin, then such arrangement of the device is known as an Ultra Thin Channel (UTC). Alternatively, in another arrangement, the device is made above a non-silicon semiconducting material layer is a Semiconductor On Insulator (SEMOI) device. The challenges in scaling the device include the need for strategies to reduce subthreshold conduction, leakage minimization in gate-oxide and junctions, reduced output conductance and transconductance, and diminishing interconnect capacitance, normalizing heat production, and other process variations & modeling complexities [2]. The issues that arise in the device's scaling involve overcoming the trade-off among the power consumption, Short Channel Effects (SCEs), and the low current. In the situation the traditional MOSFETs fail to attain, alternative device structures for further scaling have been invented. By an appropriate pursuit to the gate-metal work-function, the internal gate's threshold voltage (V_{TH1}) could be transformed to a lower compared to the external gate (V_{TH2}) with correspondingly lower the work-function of internal ϕ_{int}. Moreover, the potential profile along the channel results in depleting the broader channel region under the internal gate with drain potential variations to help simultaneously in mitigation to SCEs.

The metallic gate plays a significant role that improves the characteristics by controlling the carrier in the device channel. The metallic substance has a specific value of work-function due to inherited characteristics [3]. The work-function is a fundamental physical property that defines the least energy required to release one electron from the material surface. In the other sense, it is the minimum energy required by an electron to move up from its Fermi level [4]. Accordingly, the work-function is a prominent electronic property of any bare or coated metal. The past research has revealed that the device characteristics such as on-current improvement and the negative effect of SCE can be effectively minimized if the gate material is appropriately engineered [5]. However, gate metal engineering also tends to increase the undesired off-current; nevertheless, I_{on}/I_{off} ratio remains unaltered due to the relative increase of the on-current. Furthermore, the metal with low work-function on the drain side drops the drain bias across the region. It tends to decay in the direction of the drain end, which leads to a decline of Drain-Induced Barrier Lowering (DIBL) and channel length modulation effects.

In this research work, the authors have proposed the performance comparison of CSDG MOSFET design in a novel dual metal gate structure in stacked and unstacked arrangement

First Author and Second Author are with Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, 4041, South Africa (e-mail: abha.dargar@ieee.org, viranjay@ieee.org).

for the investigation of surface potential and electric field distribution with gate material engineering It is noteworthy that at smaller dimensions with shorter channel lengths, the device is also influenced by the confinement of energy, and the device operation is governed by the quantum-mechanical effects [6]. The channel scaling has been considered such that the quantum effects are omitted in this work.

This paper has been organized as follows: Section I introduces the background and evolution of CSDG MOSFET structure, related work, and gate meta engineering research on different Surrounding Gate (SG) structures. Section II describes the design and dimension of the proposed device structure. Section III describe the design framework and specifics of CSDG MOSFET structure for deriving the surface-potential and field profile. The comparative results and analysis of the device's electrical characteristics are given in Section IV, and Finally, Section VI outlines the conclusion of this research work and future aspects.

A. Short-Channel Effects (SCEs)

The physical gate length and the actual channel length are determined by deducting the over-all lateral diffusion of the Source and the Drain from the physical gate length. The physical gate length is much larger than the actual length; however, the difference ($Lg - L_{ch}$) cannot be computed exactly. As the actual length is scaled-down, at a certain consented point, so-called SCEs appear not to be experiential otherwise. The SCEs are abandoned in the long-channel event; nevertheless, these affect ample device performance in short-channel devices [7].

The MOSFETs at short-channel observe following significant phenomenon: (i) Two-dimensional electric field profile that results in the reduction in the threshold voltage and Drain-Induced-Barrier-Lowering (DIBL) (ii) Very high electric field strength in the channel that introduces impact ionization Hot Carrier Injection (HCI), and the breakdown and parasitic effect. (iii) The limitation imposed on electron drift characteristics brings mobility degradation and carrier velocity saturation (iv) Physical separation between the Source and the drain decreases, and it familiarizes channel length modulation and Punch-through occurrences.

B. Background and Evolution of CSDG MOSFET

As the most critical device component of modern electronics, the MOSFET has a persistent history of rigorous reforms and phenomenal scaling traced from Moore's prediction of shrinking device size and package density. The scaling of dimensions which exceeds two orders of magnitude in the past decades has undergone extensive physical modifications besides addressing the gate-control for optimum performance of the device. The rapid decrease in the device dimensions with the advent of Moore's law follows several problems such as Short-channel Effects (SCE's) and Hot Carrier Effects. In the last three decades, there have been extreme efforts to minimize the SCEs and the improved gate controllability utilizing various structural modifications. These problems have been mitigated by the introduction of multiple gates in the structure and invention of various geometries for MOSFETs such as Double-Gate (DG), Triple Gate, Omega-Gate, FinFETs, Surrounding Gate (SG), Cylindrical Surrounding Gate (CSG), and so forth [8].

The Surrounding Gate (SG) has attained much popularity among the multiple-gate structures as the gate has been exhaustively enclosed by the entire semiconductor channel, which significantly enhances the gate control over the channel. As proposed by Srivastava et al. [9], the Cylindrical Surrounding double-gate MOSFET has been one of such prominent gate-all-around devices.

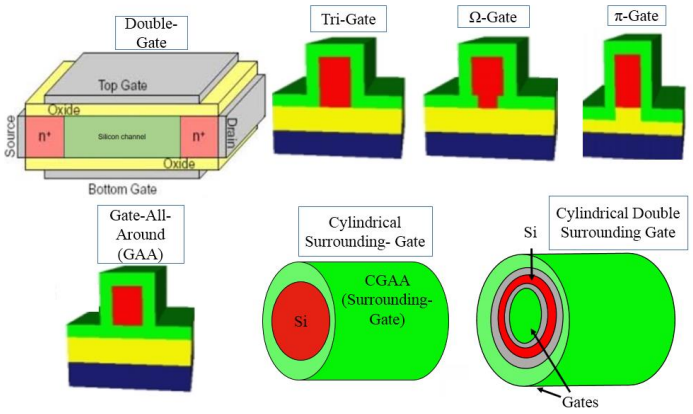

Fig. 1. Various surrounding-gate MOSFET structures.

The structure, proposed initially has been featured as two concentric cylindrical gates accommodated in a single transistor, enabling the device with improved control over the channel. In particular, the structure can be perceived as a double-gate MOSFET wrapped up from the end to end founding in a cylinder. The device's inherent characteristics, including the small-signal analysis, electrical parameters, and several other applications, have been conveyed in recent years [10].

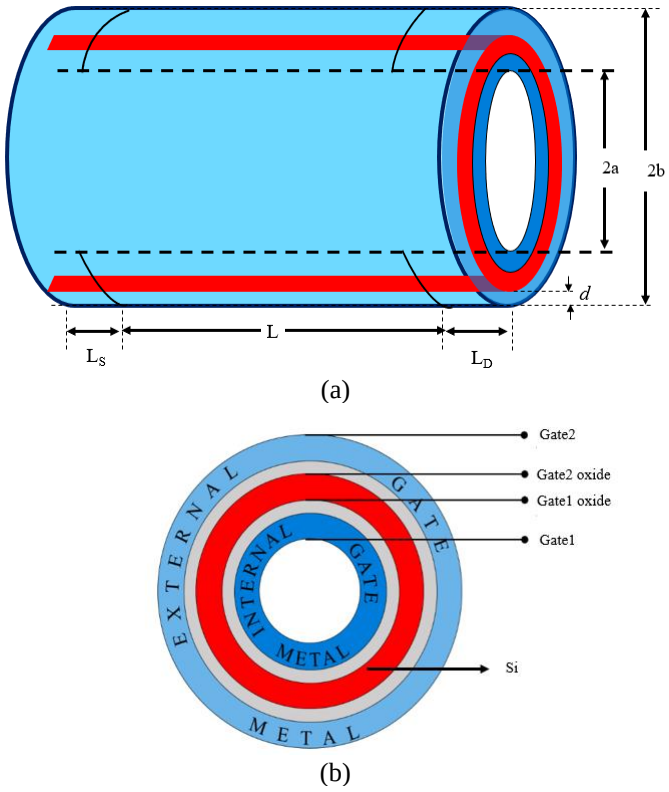

Fig. 2. Structure of CSDG MOSFET (a) schematic (b) top-view depicting internal and external gate assembly.

Past research confirms the potential of the CSDG for inventive circuits, wherein independent adjacent gates of CSDG enhances circuit design flexibility. The electrical and physical parameters analyzed at the operating conditions of a device can control the device behavior in circuit designing, which in turn results in improved performance.

C. Related work of Gate-Metal Engineering in MOSFETs

Baishya et al. (2007), in a paper, have presented a surface potential model with two material gates for DMG MOSFET of submicron scaling, assuming a varying depth of the channel depletion region caused by the difference in flat band potentials, and the deposits about the source/drain junctions. The work advised close contract and well-prediction for subthreshold current improvement based on their model comparison with the device simulator [11]. James et al. (2010) have presented a fabrication and simultaneous simulation of Double-Gate MOSFETs with different metal gate work-functions to attain the device characteristics using 2D quantum transport and Poisson equations. They reported their observation of more significant suppression of SCEs in atomic-layer deposited p-type device in terms of slighter DIBL, low subthreshold characteristics, and the improved on-off current ratio (of the order of 10^4) orders and linear increased threshold voltage with the metal gate of work-functions ranging 4.2 to 4.5 eV [12]. Ghosh et al. (2012) have proposed a metal gate-stack design in the surrounding gate structure MOSFET to demonstrate the impact of stack combinations is getting enhanced SCE immunity. The outcome presented by them ensures improved carrier transport efficiency using the stacked architecture of metal gates [13]. Pal et al. (2014) have researched on development of a model for the Dual Material Surrounding Gate MOSFET (DMSG) for the analytical treatment of electrical parameters using parabolic approximation. A good match of their model results has been reported using simulation that delivers a significant suppression of adverse short channel effects [14]. Mohapatra et al. (2014) have demonstrated a quantifiable evaluation of gate stacked double-gate MOSFET with numerical computation keeping gate metal work-functions of 4.52 eV, 4.6 eV, and 4.7 eV. The results have optimized the device dimension's gate work-function value, considering the trade-off between subthreshold slope and DIBL. Improvement in the device sensitivity and the electrical behaviors have been informed by tuning the other device parameters with the device design guideline [15].

Jouri et al. (2015), in their paper, have discussed a methodical model for the short channel tri-metal gate CSG MOSFET with high-k dielectric over SiO_2 is derived based on a center-potential solution. They showed that the high-k material in the gate-metal engineered device could surprisingly amend the impact on DIBL characteristics. Further, a trade-off between gate lengths, DIBL, and high-k material oxide has been exemplified in their work. Hui et al. (2016) have described a model for symmetrical double-material two-gate strained silicon MOSFET. The surface potential and the electric field were associated with those of a single-material device. Their work added up a deeper insight into the design with impact analysis of various device parameters.

Lagraf et al. (2019) have experimented with triple material in junction-less CSG MOSFET as an exceptional alternative of conventional MOSFET. They reported the benefit of convenient fabrication with the elimination of the p-n junctions. The impact of channel length and high-k dielectrics materials on the subthreshold features and low power optimization was reported to suggest SCE mitigation and device reliability [16]. Hasan et al. (2019) have implemented simulation to explain the modification of the work-function of gallium nitride-based DG MOSFETs to obtain the adjustment of V_{TH} shifting using simulations performance at gate-length 9.7 nm, effective oxide thickness of 0.56 nm. The most crucial observation made was the excessive suppression of SCEs using a double-gate compared to the single gate (SG) by tuning the work-function to trigger subthreshold characteristics [17].

As a device must have higher carrier transport and drive current, either a more inventive design or the modification in device physics of existing CSDG structure seems necessary. The device modification can primarily realize enhanced electrical performance in terms of the low electric field towards the drain side, surface-potential, drain current, I_{on}/I_{off}, transconductance, and input gate capacitance [18]. In the past decade, the active efforts made in work-function and gate-metal engineering on several other surrounding gate structure devices innovate the design presented in this paper.

II. Proposed Device Structure

In Cylindrical DMG design of two gates of CSDG having different work-function results in the formation of electric field maximum in channel and thereby the carrier transport efficiency increases [19, 20]. In the Stacked-DMG architecture of CSDG MOSFET, the two gates are having a combination of different work-function along the channel length as shown in Fig. 3.

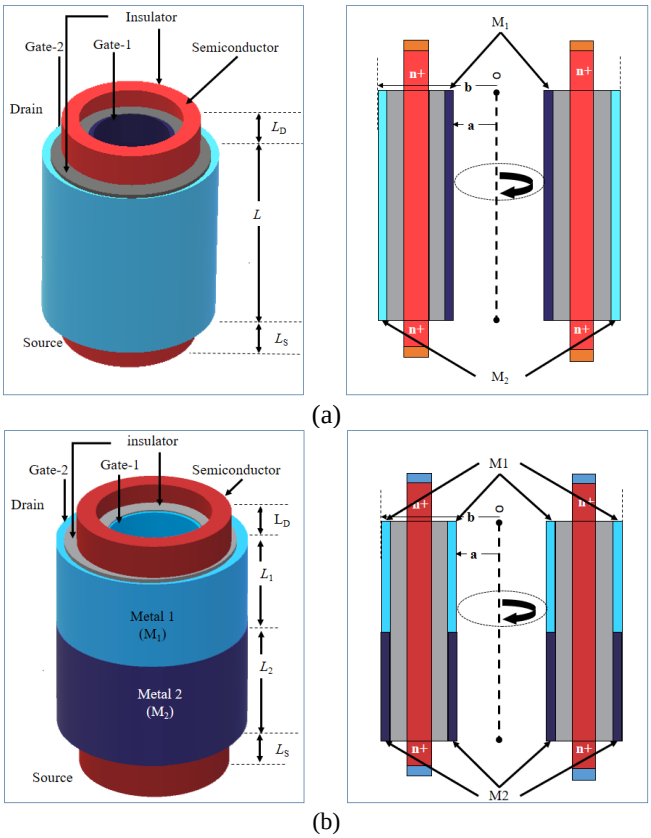

Fig. 3. Proposed schematic of cylindrical structure and 2-D cross-section in CSDG MOSFET (a) DMG CSDG (b) stacked DMG architecture.

The SiO_2 gate-dielectric is used for both the gates of the structure as it is advantageous in CMOS process. Due to the scaling of the device MOS devices, the voltage and the thickness of gate oxide get reduced. Therefore, the thickness modification is done to avoid straight tunneling leakage current using a fragile, thin layer of interface oxide that fringe the field from Source and the Drain regions.

III. Model Framework of Device Simulation

The Poisson's equation's numerical solution in two dimensions using Leibmann's iterative method defines the surface potential for an instantaneously stationary value of gate-drain voltage. The obtained solution from previous steps is needed to apply to the two-dimensional Schrödinger. The two-dimensional equation can be transformed to 1-D Schrodinger equation using the separable variation method.

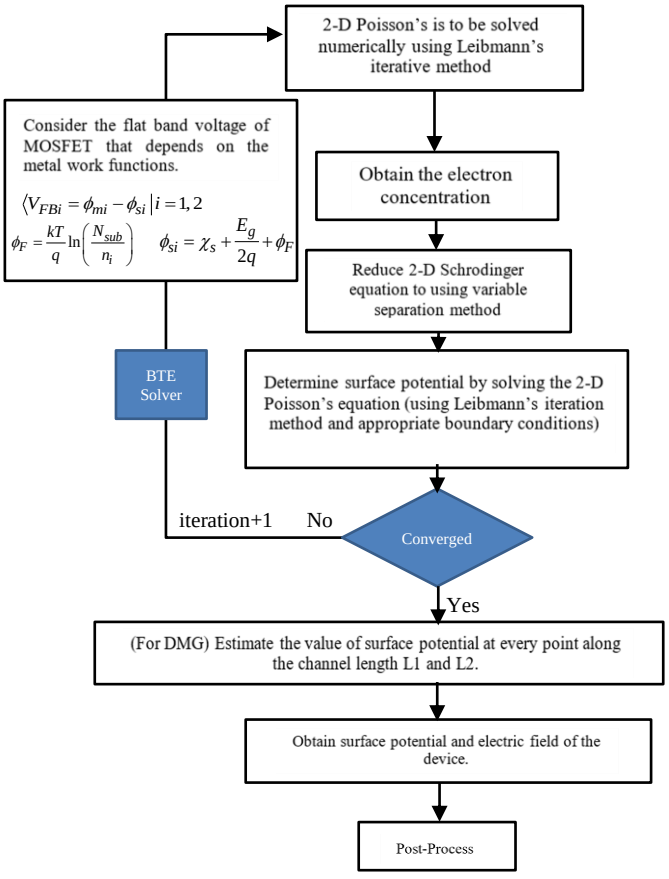

Fig. 4. Model framework for the estimation of surface potential.

As MOSFET's flat band voltage depends on the metal work-functions keeping metal work-function difference for L_1 and L_2 channel length considering each time, obtain the electron concentration. Calculate a new function in the r, z cylindrical coordinates to obtain the wavefunctions and their corresponding eigen energies, which leads to a new surface potential value in each iteration of *k* (*k* =1, 2, 3..*n*.) Calculate the relative error of the surface potential between the new values and those used in the previous iteration.

After repetition until the optimized convergence is achieved, by increasing the number of iterations of boundary condition. Table 1. list the dimensional parameters of the CSDG device in Single Material Gate (SMG), Dual Material Gate (DMG), and the stacked- Single Material Gate (stacked-DMG) structure, as comprehended in Section III. The potential at subsequent points along the channel length towards the drain end of the device is projected statistically to estimate the characteristics. The work-function of metals M_1 and M_2 of the device's DMG structure are typically chosen 4.8 eV and 4.4 eV, respectively, whereas, in a conventional structure as SMG, 4.8 eV has been deliberated as the gate metal work-function. Excepting the gate metal, other design parameters of both the SMG, DMG, and stacked-DMG are comparable.

IV. Result and Analysis

The proposed CSDG MOSFET device in SMG, DMG, and the stacked DMG structure has been simulated for obtaining the surface-potential distribution along the channel length and the electric field in the device. In the simulation structure, carrier statistics Fermi-Dirac along with the Drift-Diffusion for carrier transport, have been used to model the simplified nanoscale device.

TABLE I
LIST OF DEVICE PARAMETERS

Parameter (Unit)	Symbol	SMG	DMG	Stacked-DMG
channel length (nm)	L	20	20	20
substrate doping(cm^{-3})	N_{sub}	1×10^{17}	1×10^{17}	1×10^{17}
source-drain doping	N_D	1.6×10^{20}	1.6×10^{20}	1.6×10^{20}
gate-insulator thickness (nm)	t_{ox1}, t_{ox2}	1.5	1.5	1.5
gate metal work-function (eV)	$\phi_{m,int}$, $\phi_{m,ext}$	4.4	4.4, 4.8	4.4, 4.8
internal gate radius (nm)	a	5	5	5
external gate radius	b	12	12	12

Fig. 5 shows the result of lateral electric field distribution in dual metal and single metal gate structures of CSDG MOSFET. It is evident from Fig. 5 that the electric field tends to increase near the metal junction (L = 10 *nm*) in the DMG-CSDG structure, and that eventually results in increased carrier transport efficiency.

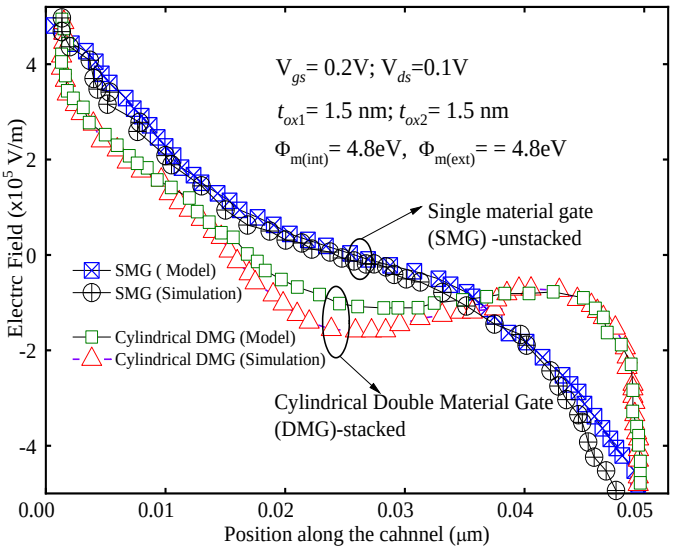

Fig. 5. Comparison of lateral electric field distribution in SMG and stacked DMG (at L_1=L_2) device structure L=20 nm, a=5 nm, b=12 nm.

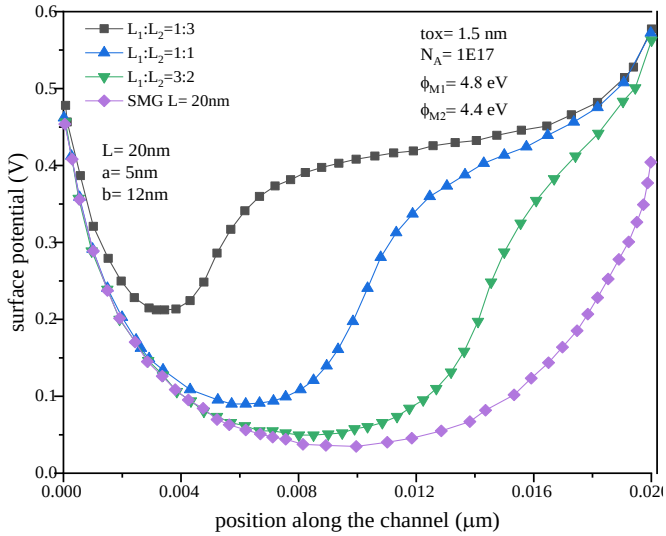

Fig. 6. Surface-potential profile versus position along the channel in DMG-CSDG device at varied region lengths at L=20 nm, a=5 nm, b=12 nm

Furthermore, the reduction of peak electric field at the drain end becomes advantageous as the high electric field at the drain side may create deleterious high-energy accelerated hot-carriers. Both the DMG and stacked-DMG structure utilizes two different metals, i.e., dissimilar work-function exists; therefore, a stride deviation in the potential near the metal interface exists. The reduced electric field in the structure specifies deterioration in the Hot Carrier Effects (HCEs). The surface-potential distribution against the normalized position along the channel is illustrated in Fig. 6.

Fig. 7 shows Surface potential as a function of position along the channel for stacked DMG-CSDG MOSFET, at Vds=0.1V and 0.2V at different oxide thickness of internal and external gates. Furthermore, it can be observed that the minima of surface-potential that lies underneath the region-1 of high work-function metal shifts towards the source side.

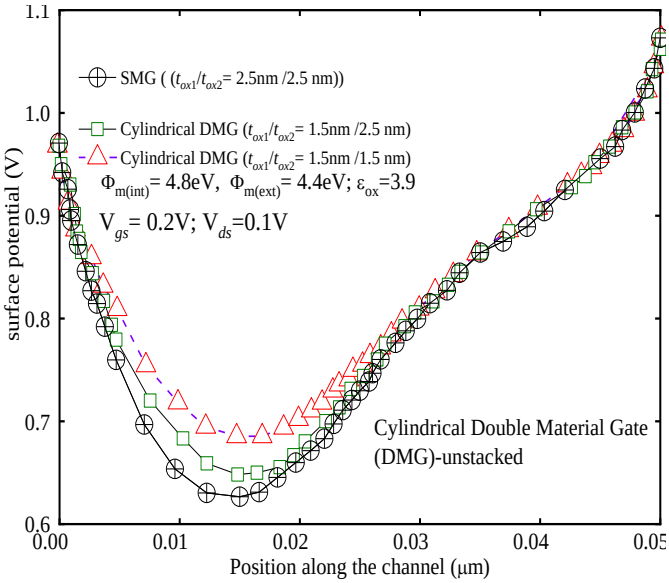

Fig. 7. Surface potential as a function of position along the channel for stacked DMG-CSDG MOSFET at different gate oxide thickness

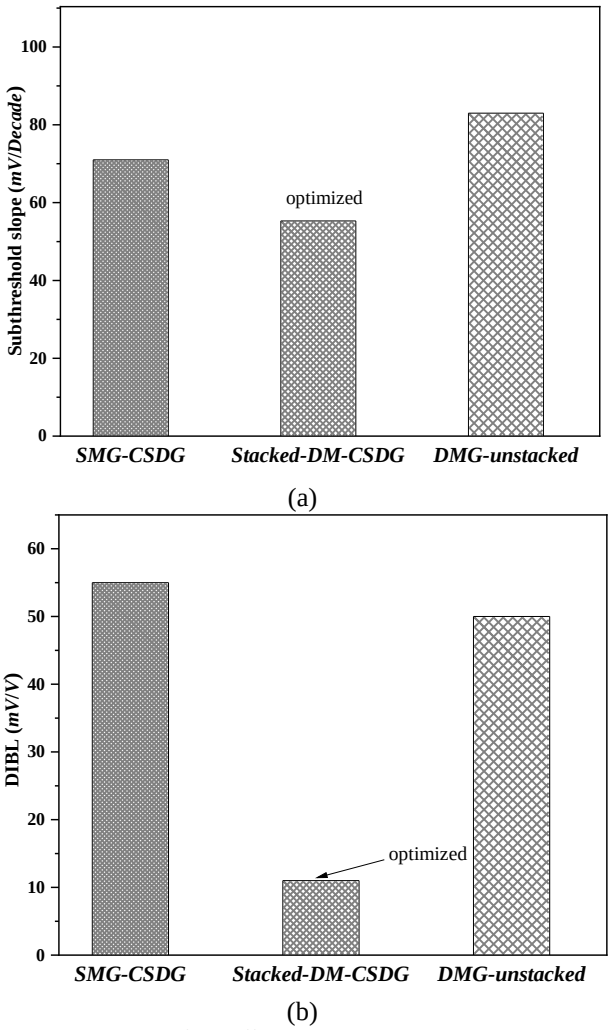

Fig. 8. Comparison of the different CSDG MOSFET SMG, DMG, and stacked-DMG structures (a) Subthreshold Swing and (b) DIBL.

It reasons the peak electric field to relocate further closer to the Source, and the uniformity of the electric field in the channel enhances. Fig. 8 shows the subthreshold and DIBL comparison of simulated device structures. The gate-stack arrangement well recognizes the improvement compared to the SMG and DMG structure of the CSDG device.

V. Conclusion and Future Work

In this paper, the authors have presented a design of CSDG MOSFET in stacked-DMG architecture. It could be established that the gate work-function is responsible for forming potential channel profile. The potential profile along the channel length results in depleting the broader channel region under the internal gate with drain potential variations to help simultaneously in mitigation to SCEs. Moreover, the channel potential minima at the different positions of metal interfaces are not the same. It is because of the high work-function of the metal headed to the source side of the channel. In stacked-DMG, the dependence of minimum surface-potential in the channel can be more effectively reduced by decreasing metal length ratios and oxide thickness ratios.

The structure comparison results are very insightful, leading to future device design improvements. Further the analysis can be extended for the performance assessment of stacked-DMG

structure incorporating the Quantum-Mechanical Effects (QMEs) in mitigating the threshold voltage shifting, Hot Carrier Effects (HCEs), and Short Channel Effects (SCEs).

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