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CHB inverter with DC-link capacitor balancing and total harmonic minimization

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Abstract: A cascaded H-bridge (CHB) multilevel inverter generally requires several DC sources. An alternative option is to replace the separate DC source feeding an H-bridge cell with a capacitor, while maintaining the other H-bridge cell with a real DC voltage source. In this paper a 7-level cascaded H-bridge inverter with a single DC-source is presented. This paper focuses mainly to achieve effective capacitor voltage balancing and selective harmonic elimination (SHE) based on the Newton Raphson algorithm (N–R). It shows hope to reduce the voltage ripple of the capacitors, which leads to higher power conversion efficiency with equal power distribution, reduces the initial cost, and complexity hence it is apt for industrial applications. Simulation results support the proposed control technique.

Key words: CHB inverter, capacitor voltage balancing, switching angles, Newton Raphson algorithm, SHE, THD

1. Introduction

Power electronic inverters can be found wherever there is a need to modify the DC electrical energy form to AC electrical form. Multilevel inverter topologies are suitable in high power applications due to their ability to synthesize waveforms with better harmonic spectrum compared with conventional two level inverters [1].

In general, multilevel converters are categorized into diode-clamped (NPC), flying capacitor (FC), and cascaded H-bridge multilevel topologies (CHB). Compared to a diode clamped and flying capacitor type [2–4], a CHB inverter requires the least number of components to achieve the same number of voltage levels [5–7].

This paper is focused on a CHB inverter, this type is based on the series connection of several H-bridge cells. Each HB cell must be fed by a stiff voltage source. The CHB multilevel

converter has been applied in high-power and high-quality applications such as active filters, reactive power compensators, photovoltaic power conversion [8], and electric-drive vehicles in which the traction motor is driven by batteries [9].

In earlier configurations, every one of these DC-sources had to contribute to the overall power supplied to the load. Recently, it was demonstrated that under certain operating modes, it is possible to replace one of these sources with energy storage devices, e.g. capacitors. In other words, the entire power can be supplied by only one DC-source. This approach benefits from cost reductions [10].

Balancing the voltages across the replacing capacitor turns out to be a key issue. In this regard a switching control technique is presented, in order to achieve the replacing capacitor voltage balancing while ensuring selective harmonic elimination.

In this paper, the operating modes under which both the capacitor voltage balancing and the lower harmonic order are obtained are analytically investigated and simulated.

The method used to switch cascaded H-bridge cells can be based either on the fundamental switching frequency, i.e. staircase modulation, or the pulse width modulation (PWM) technique [11]. In the fundamental switching frequency approach, the switching losses are less, but the harmonics in the output voltage waveform appear at lower frequencies. Several methods are proposed in the literature to selectively eliminate harmonics in the output waveforms of multilevel converters [1, 12, 13].

In this paper, selective harmonic elimination (SHE) is suggested for a 7-level CHB inverter with a single DC-source. The Newton-Raphson method [14–16], is used to calculate switching angles with the capability to eliminate the lowest order harmonics (5^{th} and 7^{th}), while ensuring capacitor voltage balancing.

FPGAs are digital hardware-based devices and they have become an increasingly popular technology in digital prototyping for multilevel inverters due to their speed and flexibility [17].

The analytical results are validated through simulation results. The analytical and simulation results based on N–R optimization prove the effectiveness of the proposed approaches.

This paper is organized as follows: section 2 describes the power topology of the cascade multilevel inverter with the DC single source, the capacitor voltage balancing and harmonic elimination are explained in section 3, simulation results are presented in section 4. Finally, the concluding remarks are drawn in section 5.

2. 7-level CHB inverter with single DC-source

In a CHB multilevel inverter each unit has its own separated DC source, when the DC-link voltages of HBs are identical, it is called a symmetrical multilevel inverter [18].

However, it is possible to have different values among the DC-link voltages of HBs, and the circuit called an asymmetrical multilevel inverter [19]. Figure 1 shows the circuit topology of the CHB inverter with a single DC source. However, we demonstrate in this section that only the first cell needs to be supplied by a real DC power source, while the second cell can be supplied with a capacitor replacing its DC link [20].

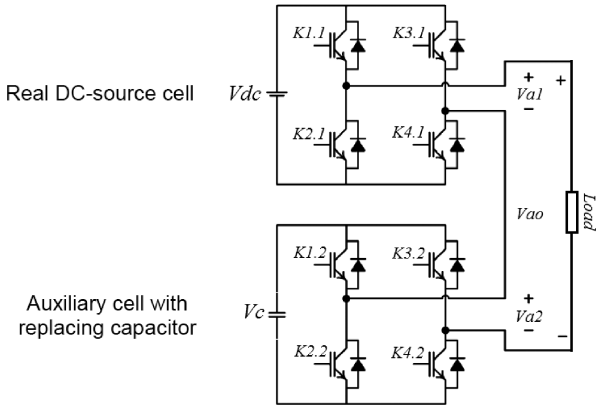
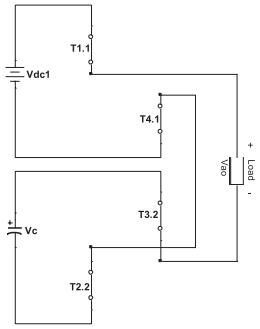


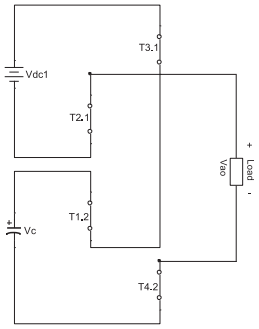
Fig. 1. Power topology of CHB inverter with single DC-source

The outputs of the H-bridge cells are connected in series such that the entire output voltage waveform is the sum of the individual cell outputs. The output voltage can be given by:

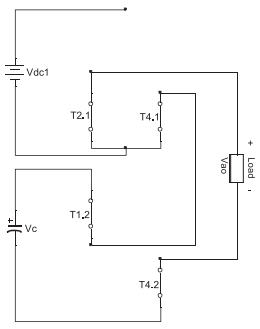
$$V_{a1} + V_{a2} = V_{ao}\,, \tag{1}$$



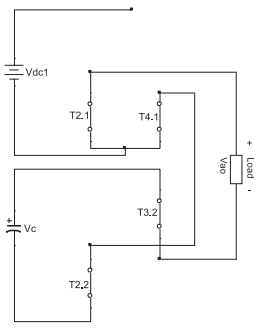
Capacitor charge: $V_{ao} = V_{dc} - V_c$



Capacitor charge: $V_{ao} = -V_{dc} + V_c$



Capacitor charge: $V_{ao} = +V_c$



Capacitor charge: $V_{ao} = -V_c$

Fig. 2. Capacitor charge / discharge states

where V_{a1} and V_{a2} are the output voltages in the real DC-source cell and auxiliary cell with the replacing capacitor, respectively.

Figure 1 shows that the proposed inverter can be operated in the asymmetrical mode when $V_{dc1} = V_{dc}$ and $V_c = V_{dc}/2$ in order to obtain 7-level output voltage.

The output voltage level V_{ao} at $V_{dc}/2$ can be generated in two ways, to choose $V_{a1} = V_{dc}$ and $V_{a2} = -V_{dc}/2$, in this case, V_c will be charged for negative output currents. The second way is to choose $V_{a1} = 0$ and $V_{a2} = V_{dc}/2$, in this case, V_c will be discharged for negative output currents. As a result we must choose the first way in which the capacitor voltage will be charged.

A similar argument can be made when the desired output voltage is $-V_{dc}/2$. In this case, we must choose $V_{a1} = -V_{dc}$ and $V_{a2} = +V_{dc}/2$ in which V_c will be charged for positive output currents. Therefore, the output voltage V_{ao} will have 7-levels as illustrated in Figure 3.

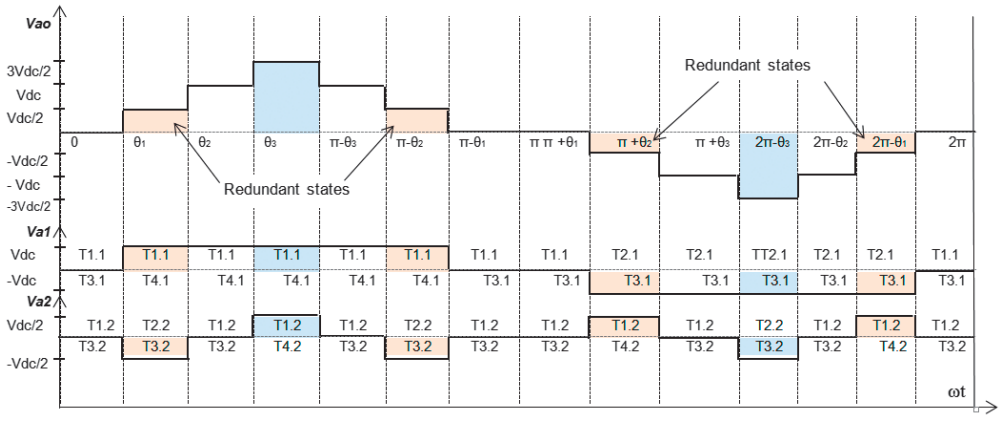
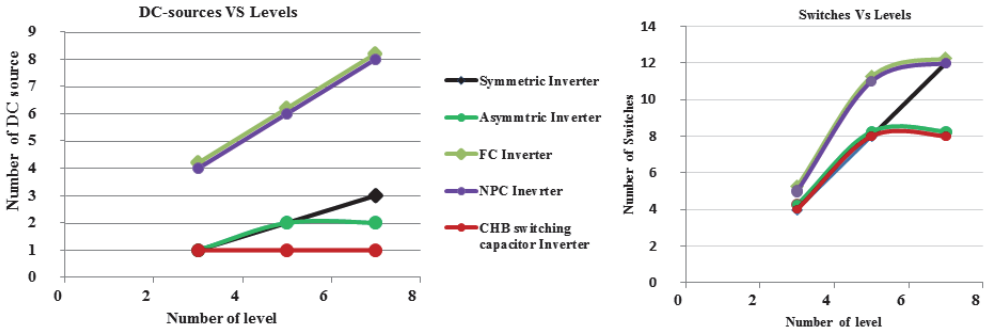


Fig. 3. Staircase CHB multilevel inverter output voltage

The single DC-source inverter (SDCS) topology is compared with the conventional NPC, FC and CHB inverter topologies [19, 20] and [2, 4]. The comparison, shown in Figure 4(a) and Figure 4(b), is done in view of optimizing the number of used DC-sources with an increasing



(a) (b)

Fig. 4. (a) variation of DC-source versus levels; (b) variation of DC-source versus levels

number of levels in the output voltage and the number of switches as a result of the number of driver circuits. Figure 4(a) shows that the CHB inverter with the switched capacitor can achieve the same number of levels generated by the mentioned inverters with a minimum number of DC-sources. Figure 4(b) reveals the fact that the SDCS inverter, for both symmetric an asymmetric configuration, is the one with the minimum number of switches.

It is clear from comparison results that the SDCS cascaded multilevel inverter is able to generate a higher number of output levels with a lower number of power switches (IGBTs/MOSFETs), driver gate circuits and DC voltage sources than the conventional inverters topologies.

3. Capacitor voltage balancing considering THD minimization

In this section, the objective is to control the single phase 7-level inverter's commutation switches, while ensuring capacitor voltage balance and eliminating 5^{th} and the 7^{th} harmonic order.

3.1. Voltage balancing

The existence of redundant switching states has been assumed to be adequate for capacitor voltage balancing.

For the following demonstrations, V_{dc} is considered to be the value of a real DC-source and the replacing capacitor is chosen to be initially charged, $V_{dc1} = V_{dc}$, $V_c = V_{dc}/2$, $\omega = \pi f$ and $\tau = RC$. The objective is to regulate the capacitor voltage at $V_{dc}/2$. Below, we develop an analytical study of the capacitor voltage according to the switching angles. To achieve capacitor voltage balancing, we present in this section the single phase capacitor voltage evolution $V_c(\omega t)$ according to the switching angles θ_1, θ_2 and θ_3, while assuming that the initial voltage of the capacitor $V_c(0) = V_{dc}/2$. The switch states sequences are presented in Table 1.

Since the charging and discharging patterns are repeated every half of the period, examining only one half is adequate. The first half of the period is divided into seven subintervals and the voltage level of the capacitor is investigated in each subinterval (see Figure 3). Only the subintervals $[\theta_1 - \theta_2]$, $[\theta_3 - \pi - \theta_3]$ and $[\pi - \theta_2, \ldots, \pi - \theta_1]$ are involved in the charge and discharge equations.

During subinterval $[\theta_1 - \theta_2]$, we can express the capacitor voltage as:

$$V_C(\theta_1) = \frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right) = \frac{E}{2}\left(2 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right). \tag{2}$$

The capacitor voltage in subinterval II has increased by:

$$\Delta V_C(\text{II}) = \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right). \tag{3}$$

During subinterval $[\theta_3 - \pi - \theta_3]$ the capacitor voltage has decreased by:

$$\Delta V_C(\text{IV}) = -V_{dc} + V_{dc} \times e^{-\frac{\pi-2\theta_3}{\omega\tau}} - \frac{V_{dc}}{2} e^{-\frac{\pi+\theta_2-\theta_1-2\theta_3}{\omega\tau}} + \frac{V_{dc}}{2} e^{-\frac{\theta_2-\theta_1}{\omega\tau}}. \tag{4}$$

Table 1. Capacitor voltage states

Subinterval	HB 2 capacitor voltage state	Subinterval capacitor final value: $Vc(\omega t)$	V_{a1}	V_{a2}
I: $0 < \omega t < \theta_1$	no capacitor charge or discharge	$\frac{V_{dc}}{2}$	0	0
II: $\theta_1 < \omega t < \theta_2$	capacitor charge	$\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right)$	V_{dc}	$-V_{c(\omega t)}$
III: $\theta_2 < \omega t < \theta_3$	no capacitor charge or discharge	$\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right)$	V_{dc}	0
IV: $\theta_3 < \omega t < \pi - \theta_3$	capacitor discharge	$\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right)\left(e^{-\frac{\pi-2\theta_3}{\omega\tau}}\right)$	V_{dc}	$V_{c(\omega t)}$
V: $\pi-\theta_3 < \omega t < \pi-\theta_2$	no capacitor charge or discharge	$\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right)\left(e^{-\frac{\pi-2\theta_3}{\omega\tau}}\right)$	V_{dc}	0
VI: $\pi-\theta_2 < \omega t < \pi-\theta_1$	capacitor charge	$\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right)\left(e^{-\frac{\pi-2\theta_3}{\omega\tau}}\right)\left(1 - e^{-\frac{\theta_1-\theta_2}{\omega\tau}}\right)$	V_{dc}	$V_{c(\omega t)}$
VII: $\pi - \theta_1 < \omega t < \pi$	no capacitor charge or discharge	$\frac{V_{dc}}{2} + \frac{V_{dc}}{2}\left(1 - e^{-\frac{\theta_2-\theta_1}{\omega\tau}}\right)\left(e^{-\frac{\pi-2\theta_3}{\omega\tau}}\right)\left(1 - e^{-\frac{\theta_1-\theta_2}{\omega\tau}}\right)$	0	0

In subinterval $[\pi - \theta_2, \ldots, \pi - \theta_1]$ capacitor charges, ΔV_c as follows

$$\begin{aligned}\Delta V_C(\mathrm{VI}) = &- V_{dc} - V_{dc} \times e^{-\frac{\theta_2-\theta_1}{\omega\tau}} + 2V_{dc} \times e^{-\frac{\pi+\theta_2-\theta_1-2\theta_3}{\omega\tau}} - \\ &- \frac{V_{dc}}{2} e^{-\frac{\pi+\theta_2-2\theta_1-2\theta_3}{\omega\tau}} - 2V_{dc} e^{-\frac{\pi-2\theta_3}{\omega\tau}} + \frac{V_{dc}}{2} e^{-\frac{\pi+\theta_2-\theta_1-2\theta_3}{\omega\tau}},\end{aligned} \tag{5}$$

$$\Delta V_C(\mathrm{VI}) = \Delta V_C(\mathrm{II}). \tag{6}$$

In order to achieve capacitor voltage balancing, the capacitor discharge in subintervals IV must be less than the capacitor charge in subintervals II and VI.

$$|\Delta V_C(\mathrm{IV})| \leq |\Delta V_C(\mathrm{II})| + |\Delta V_C(\mathrm{VI})|. \tag{7}$$

3.2. SHE based on Newton Raphson algorithm

The selective harmonic elimination control technique [14–16], for the proposed SDCS 7-level inverter considering a minimum THD is discussed in this subsection. A more practical approach to THD reduction is the elimination of selected harmonic orders, by choosing the switching angles strategically. In high power applications, eliminating a low order harmonic completely would eliminate the need for the otherwise required filtering equipment required for that particular order.

The inverter output voltage V_{ao} waveform, can be expressed in the Fourier series as, [21–23].

$$V_{ao}(\omega t) = B_0 + \sum_{n=1}^{+\infty} B_n \cos(n\omega t) + A_n \sin(n\omega t). \tag{8}$$

The even harmonics are also absent due to the quarter-wave symmetry [24].

$$V_{ao}(\omega t) = \sum_{n=1}^{+\infty} A_n \sin(n\omega t), \tag{9}$$

where, A_n is the magnitude of the n^{th} harmonic order, such as:

$$A_n = \frac{4V_{dc1}}{2n\pi} \sum_{i=1}^{P} \cos(n\theta_i). \tag{10}$$

In the staircase output voltage waveform, the number of the switching angles to be calculated is given by P:

$$P = \frac{\text{Number of levels} - 1}{2}. \tag{11}$$

Lower order harmonics produce high harmonic content (THD) in the output voltage and current. It is desirable to control the fundamental component of the output voltage at a certain value and eliminate the low-order harmonics as much as possible [25].

In our case, the three switching angles θ_1, θ_2 and θ_3 must be determined to eliminate the first two odd non triple harmonic components (5^{th} and 7^{th}). In a balanced three-phase and four-wire system, the triple-n harmonics will be automatically eliminated. One solution approach for sets of a nonlinear transcendental system of Equations (12) is by applying an iterative method based on the Newton Raphson algorithm.

$$\left.\begin{aligned} &\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = 3M \\ &\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \\ &\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \end{aligned}\right\}. \tag{12}$$

Assuming that the expression of the modulation index $\boldsymbol{M}$ is given by:

$$\boldsymbol{M} = \frac{2A_1\pi}{4PV_{dc1}}, \qquad (0 < \boldsymbol{M} < 1). \tag{13}$$

Switching angles θ_1, θ_2 and θ_3 must satisfy the following condition:

$$\theta_1 \leq \theta_2 \leq \theta_3 \leq 90^{\circ}. \tag{14}$$

The N–R method based on harmonic elimination and capacitor voltage balancing is described by the flow chart given in Figure 5.

To provide THD and capacitor voltage fluctuation minimization, a system of Equations (15) is given, this equation includes the first three equations in the same system which are used to solve

the problem of switching angles. The last equation presents the voltage fluctuation constraint.

$$\left.\begin{aligned} &\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=3M \\ &\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)=0 \\ &\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)=0 \\ &\{|\Delta V_C(\mathrm{IV})|\le|\Delta V_C(\mathrm{II})|+|\Delta V_C(\mathrm{VI})| \end{aligned}\right\}. \tag{15}$$

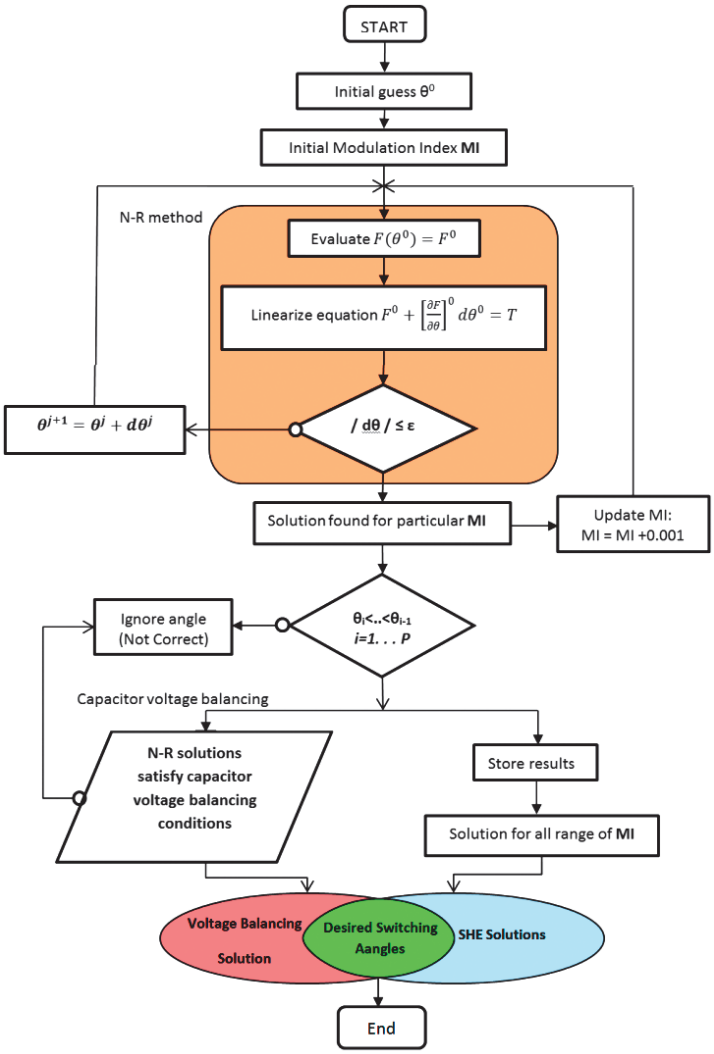
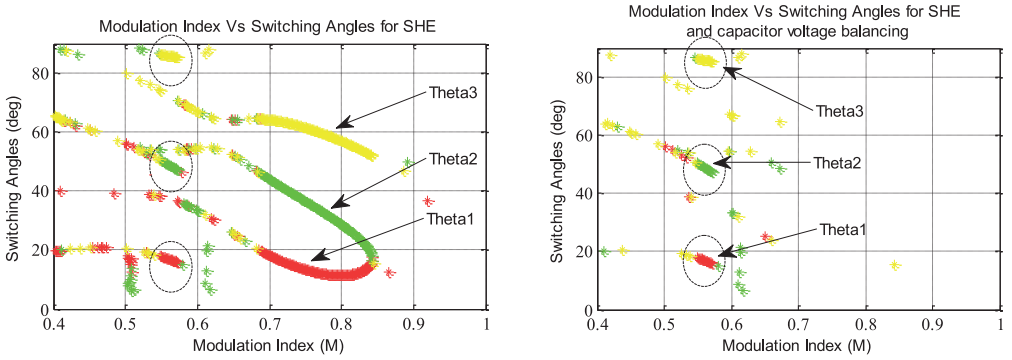


Fig. 5. SHE and capacitor voltage balancing based on N–R algorithm flow chart

4. Simulation results

Figure 6(a) and Figure 6(b) given below are obtained by using Matlab programming based on Newton Raphson, Figure 6(a) presents the graph drawing for the three angles θ_1, θ_2 and θ_3 at various modulation index $\boldsymbol{M}$. Figure 6(b) presents θ_1, θ_2 and θ_3 at various values $\boldsymbol{M}$ considering capacitor voltage balancing conditions.



(a) (b)

Fig. 6. (a) Switching angles versus modulation index based on N–R algorithm capacitor voltage balancing; (b) switching angles versus modulation index based on N–R algorithm for SHE

These graph drawings allow us to choose the modulation index which verifies Equations (7) and (12) of system (15), for which θ_1, θ_2 and θ_3 eliminate the 5^{th} and 7^{th} harmonics and verifies capacitor voltage balancing.

Based on MATLAB/Simulink, a single phase 7-level inverter is used to drive a resistive load ($R = 50\ \Omega$) such as the first HB inverter unit (HB1) DC source voltage equals 100 V, HB2 capacitor voltage equals 50 V with a capacitor value C of 10 mf.

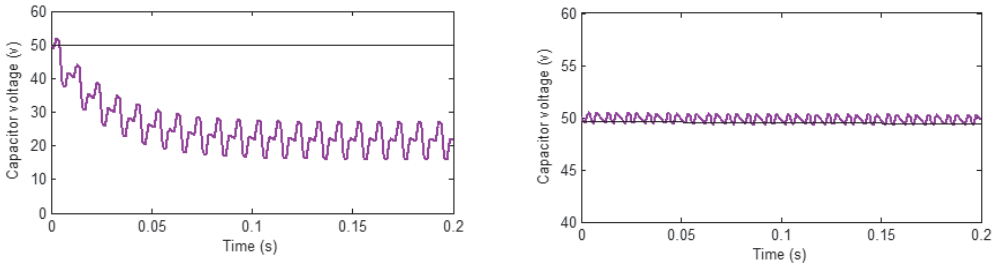
The modulation index is chosen to be $\boldsymbol{M} = 0.57$, the corresponding switching angles are: $\theta_1 = 16.14°$, $\theta_2 = 47.31°$ and $\theta_3 = 85.69°$.

In the case of equal calculating switching angles (ECSA), which is based on the application of control signals with identical switching angles, the voltage of the capacitor will decrease continuously. Therefore one cannot regulate the capacitor voltage in this case.

Based on the simulation result of Figure 6, the HB2 capacitor voltage is balanced, and the predictions of (7) and (12) on capacitor voltage balancing agree with the analytical results.

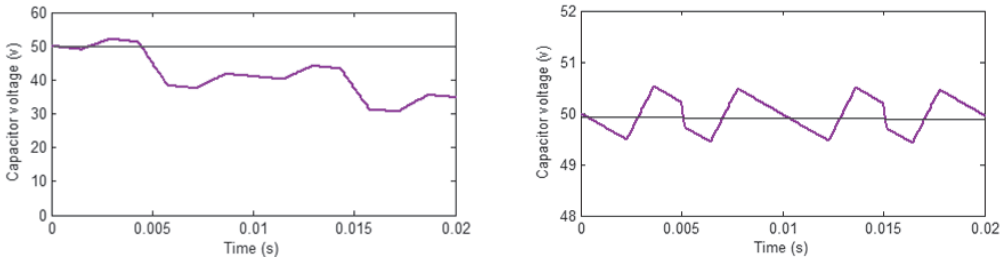
Figure 12(b), shows that for the chosen modulation index and angles ($\boldsymbol{M} = 0.57$, $\theta_1 = 16.14°$, $\theta_2 = 47.31°$ and $\theta_3 = 85.69°$), the desired 7-level inverter output voltage is obtained, and the 5^{th} and 7^{th} are eliminated compared with the ECSA method showed in Figure 12(a).

As shown in Figure 11, for a multilevel inverter with an N-level we can only choose $((N-1)/2)-1)$ harmonics to be eliminated, this is why we are obliged to select two harmonics to be eliminated, $((7-1)/2)-1 = 2)$, in this paper. In the system of non-linear Equations (15), 5^{th} and 7^{th} harmonic orders, are chosen for SHE for the reason that they are the most troublesome,



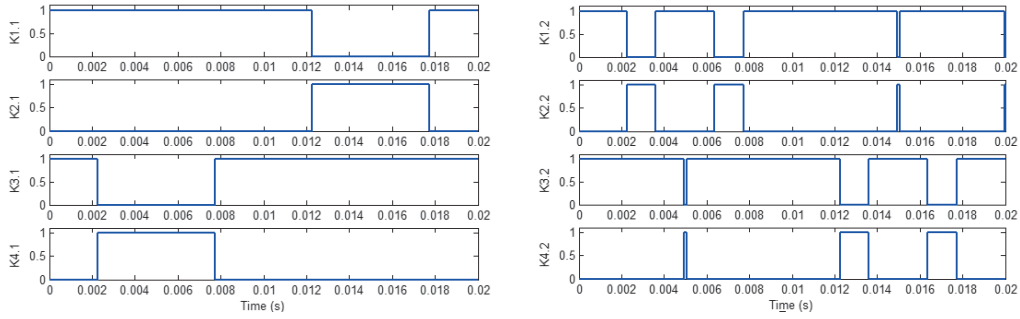
(a) (b)

Fig. 7. Capacitor voltage V_c: (a) based on ECSA; (b) based on N–R algorithm



(a) (b)

Fig. 8. An enlarged view of the capacitor voltage versus time: (a) based on ECSA; (b) based on N–R algorithm



(a) (b)

Fig. 9. 7-level inverter control signals based on N–R algorithm: (a) main cell; (b) auxiliary cell

which affects the THD (even harmonics are absent and triple harmonic order will be automatically eliminated in a three phase system).

The objective here is achieved by minimizing THD (26% for ECSA to 20% for N–R method) without using any additional circuit (e.g.: filters).

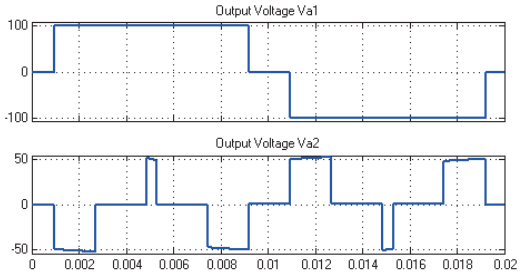
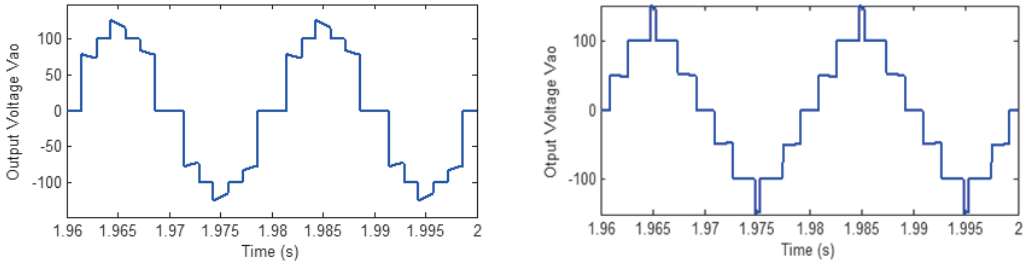
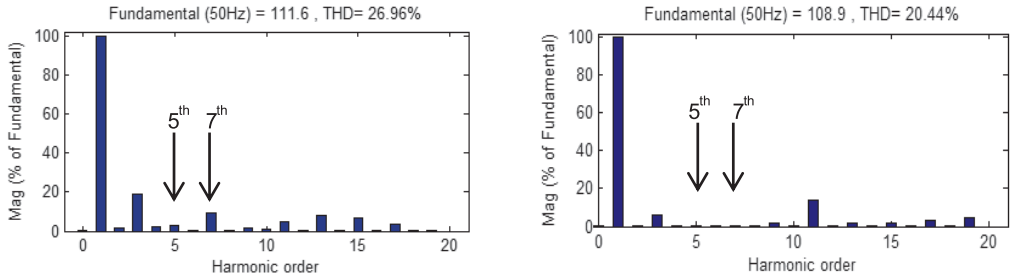


Fig. 10. Output voltage waveform for V_{a1} and V_{a2}



(a) (b)

Fig. 11. SDCS 7-level inverter output voltage waveform (V_{ao}): (a) based on ECSA; (b) based on N–R algorithm



(a) (b)

Fig. 12. FFT analysis for the 7-level output voltage waveform (V_{ao}): (a) based on ECSA; (b) based on N–R algorithm

5. Conclusion

The single DC source cascaded H-bridge inverter was investigated in this paper. The Newton-Raphson technique has been used to obtain the optimum switching angles to eliminate 5^{th} and 7^{th} harmonic and to balance the replacing capacitor voltages. The simulation results agree with

the analytical results. The results show that the balancing of the capacitor voltage is achievable with minimizing the total harmonic distortion.

Generally, in the literature, a balancing capacitor and harmonic minimization are not the same criteria. In this work these two objectives are combined in order to find a condition which allows the reduction of components (DC source) when using a capacitor and allows for an output harmonic profile improvement.

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