

A novel in-phase disposition SPWM pulse allocation strategy for cascaded H-bridge inverter

Yonggao Zhang¹, Jian Xiong^{1,2}, Lingtao Kong¹, Xiaochen Wang¹

¹ School of Electrical and Automation Engineering
East China Jiaotong University, Nanchang, China
e-mail: ygzhang@ecjtu.jx.cn

² Zhuzhou CRRC Times Electric Co., Ltd., Zhuzhou, China
e-mail: xj0791@foxmail.com

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Abstract: A novel in-phase disposition (IPD) SPWM pulse allocation strategy applied to a cascaded H-bridge (CHB) converter is presented in this paper. The reason causing the power of the CHB converter imbalance is analyzed according to the traditional structure, the conception of power imbalance degree is introduced and the principle of the novel in-phase disposition SPWM allocation strategy is deduced in detail. The new pulse allocation scheme can ensure the power balance in 3/4 cycles through interchanging the PWM pulse sequence of the different CHB cell, meanwhile it makes the full advantage of the IPD control strategy, lower the total harmonic distortion (THD) of line voltage compared to a carrier phase shifted (CPS) control strategy, which is verified by theoretical derivation. A seven-level cascaded inverter composed by three H-bridge cells is taken as the example. The simulation and experiment is performed. The results indicate the validity of the analysis and verify the effectiveness of the proposed SPWM allocation strategy.

Key words: in-phase disposition SPWM, Inverter, CHB, THD

1. Introduction

A cascaded multilevel inverter can be described in 3 forms: a diode-clamped inverter, flying-capacitor inverter and CHB inverter, which are widely used in a high power transmission system [1–3]. There are switch redundancy and dc source redundancy in the cascaded inverter. That is to say it has the advantages of lower voltage stress, a higher level of voltage output, lower switch frequency and lower voltage regulation compared with a typical inverter. The CHB inverter is commonly used in a photovoltaic power generation system because it needs independent power supply [4]. A modular multilevel converter (MMC) inherits the structure advantage of the CHB, which is extensively used in the MMC-HVDC system [5].

IPD, as a modulation strategy applied in multilevel inverters, is getting more and more attention because of its low line voltage THD. However, the IPD cannot achieve power balance for its inherent vice [6–8]. To solve this problem, paper [9] adopted a pulse rotation control strategy based on the IPD to achieve power balance in a single cycle. Paper [10] proposed a random PWM allocation of the cascaded inverter, with the inverter working longer, the usage rate of each unit is going to be the same. However, this method needs a long time to achieve power balance, so it gets worse when switching the working state frequently. Paper [11] proposed that increasing carrier frequency when a modulation ratio is low, but some pulse of the switch cannot be triggered for a low modulation ration. It causes that some units have no voltage output, so this method is faulty. Papers [12–13] improved the conventional in-phase disposition PWM method to achieve the balance of the flying capacitor through adding the link of selection of zero level which will be a reasonable allocation of zero level vectors. The carrier waveform will change with different modulations.

This paper proposed a novel IPD SPWM allocation strategy that ensures the power balance in 3/4 cycles through an interchanging trigger signal of the CHB cells, while making the full advantage of the IPD control strategy and lowering the THD of line voltage compared to the CPS. This paper also analyzes the influence factors of power imbalance. In the new scheme the time when the power balance is achieved is not only shorter, but also suitable for the condition of a low modulation ratio. Finally, the simulation and experiment are performed, and the results indicate the validity of analysis.

2. IPD control strategy for CHB

Fig. 1 shows the structures of an m -level CHB inverter. The topology consists of multiple single-phase H-bridge cells in series to synthesize a higher level output. H-bridge cell's power is supplied by independent voltage source E .

The inverter phase voltage can be found from

$$V_p = V_{Hp1} + V_{Hp2} + V_{Hp3} + \dots + V_{Hpn}. \quad (1)$$

In the formulas, $p = a, b, c$. V_{Hp} is the p phase voltage; V_{Hpn} is the n -th H-bridge cell voltage of the p phase. Each H-bridge cell can output 3-level voltage, $0, \pm E$, which makes voltage synthesizing flexible.

Taking the phase as an example, the schematic diagram of the IPD should be shown as in Fig. 2.

Fig. 2a shows the relationship of a modulation wave and triangular carriers. According to the IPD modulation, an m -level CHB inverter using the IPD modulation scheme requires $(m-1)$ triangular carriers. As for a 7-level inverter, it require 6 triangular carriers, all having the same frequency and amplitude. The 6 triangular carriers are vertically disposed such that the bands they occupy are contiguous. The uppermost and lowermost carrier pair, v_{cr1} and v_{cr1-} , are used to generate the gating signals for upper switches S_{11} and S_{31} in H-bridge cell H_{a1} of Fig. 2a, other carrier pairs are similar. The gate signals for the lower switches in each H-bridge are complementary to their corresponding upper switches, and thus for simplicity they are not shown.

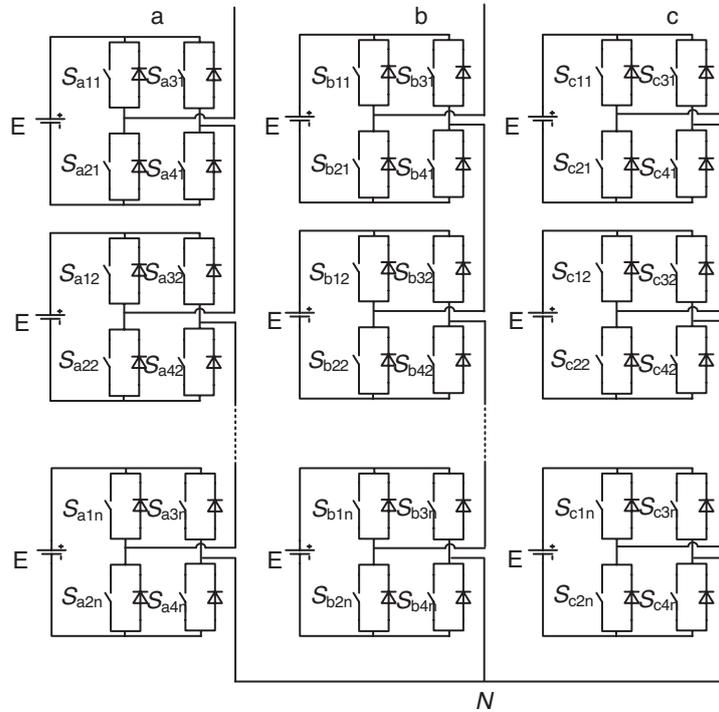


Fig. 1. Topology of cascaded m -level cascaded H-bridge inverter

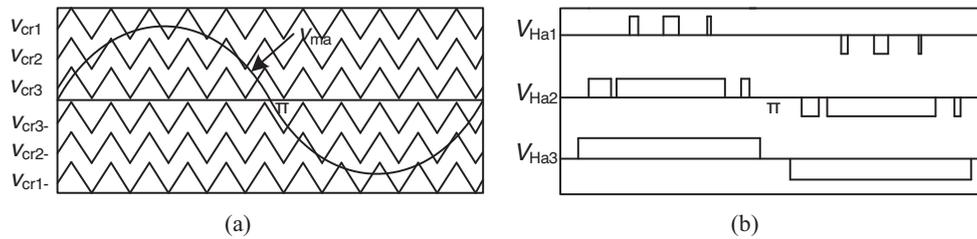


Fig. 2. The schematic diagram of IPD: the modulation wave and carrier waves (a); cell voltage of a phase (b)

Fig. 2b shows output voltage of a phase H-bridges cells. For the carriers above the zero reference (v_{cr1} , v_{cr2} and v_{cr3}) the switches S_{11} , S_{12} , S_{13} are turned on when the phase a modulating signal v_{ma} is higher than the corresponding carriers. For the carriers below the zero reference (v_{cr1-} , v_{cr2-} and v_{cr3-}) the switches S_{31} , S_{32} , S_{33} are switched on when the phase a modulating signal v_{ma} is higher than the corresponding carriers. So, the time sequence of cell voltage V_{Ha1} is consistent with the stack of gate signals, S_{11} and S_{31} . The conclusion can be made that the cell voltage sequence reflects device frequencies and conduction time. The switches in H_{a1} and H_{a2} are turned on and off three times per cycle, but the conduction time of them is not equal, however

the switches in H_{a3} are only turned on and off once per cycle. Furthermore, it makes the output power and cell losses unbalanced among cells H_{a1} , H_{a2} , H_{a3} .

To clarify the essence of power imbalance, this paper analyses the relationship between output power and cell losses.

Defining the power unbalance degree (PUD) function as:

$$S(\alpha, \beta) = \left[1 - \frac{\min(t_{Hp\alpha}, t_{Hp\beta})}{\max(t_{Hp\alpha}, t_{Hp\beta})} \right] + i \left[1 - \frac{\min(n_{Hp\alpha}, n_{Hp\beta})}{\max(n_{Hp\alpha}, n_{Hp\beta})} \right], \quad (t \in T), \quad (2)$$

where, T is the reference period, $t_{Hp\alpha}$, $t_{Hp\beta}$ are, respectively, the conduction time of cells $H_{p\alpha}$ and $H_{p\beta}$ in T , $n_{Hp\alpha}$, $n_{Hp\beta}$ are, respectively, the switching times of cells $H_{p\alpha}$ and $H_{p\beta}$ in T . $H_{p\alpha}$, $H_{p\beta}$ are two cascaded H-bridge cells of the p ($p = a, b, c$) phase. The real part is determined by conduction time difference and imaginary part is determined by switching times difference. The greater the difference is, the greater $S(\alpha, \beta)$ is. The maximum of the real part or imaginary part is one.

Because the cell voltage waveforms in Fig. 2b are central symmetry, the device conduction time and switching times within the first half-cycle are equal to those within the second half-cycle. From 0 to π , the output power of the cell can be expressed as:

$$P_{Hp\alpha} = UI_p = EI_p \sqrt{\frac{2t_{Hp\alpha}}{T}}. \quad (3)$$

In this equation U and I_p present the cell voltage effective value and phase current effective value. Here, T is equal to one cycle, $2\pi/\omega$, where ω is the angular frequency. Once the circuit parameters are defined, output power $P_{Hp\alpha}$ of cell $H_{p\alpha}$ is proportional to its corresponding square root of conduction time $t_{Hp\alpha}$. If $t_{Hp\alpha}$ is equal to $t_{Hp\beta}$, the real part of e.g. (2) $\text{Rm}[S(\alpha, \beta)]$ is equal to 0 and the output power of cell $H_{p\alpha}$ must be equal to that of cell $H_{p\beta}$.

Cell losses include conduction losses and switching losses. A cell output voltage, by controlling two switches, turn them on and off simultaneously, which causes double conduction losses and four times switching losses in a half cycle. From 0 to π , cell losses can be expressed as:

$$E_{Hp\alpha} = 2t_{Hp\alpha}w_{Hp\alpha} + 4n_{Hp\alpha}k_{Hp\alpha}, \quad (4)$$

where, $w_{Hp\alpha}$ and $k_{Hp\alpha}$ are, respectively, the average device conduction losses and average switching losses of cell $H_{p\alpha}$. According to e.g. (3), if $t_{Hp\alpha} = t_{Hp\beta}$, then $P_{Hp\alpha} = P_{Hp\beta}$. The effective values of cells $H_{p\alpha}$, $H_{p\beta}$ are U , and their corresponding cell current effective value is also equal to I_p . So, $w_{Hp\alpha}$ is, approximately, equal to $w_{Hp\beta}$ and $k_{Hp\alpha}$ is, approximately, equal to $k_{Hp\beta}$. If $t_{Hp\alpha} = t_{Hp\beta}$ and $n_{Hp\alpha} = n_{Hp\beta}$, $H_{p\alpha}$, $H_{p\beta}$ can both achieve cell loss balance and power imbalance degree is 0. Therefore, $S(\alpha, \beta) = 0$ is the necessary and sufficient condition of the power balance. The relationship between Equation (2), Equation (3) and Equation (4) can be expressed as:

$$S(\alpha, \beta) = 0 \Leftrightarrow E_{Hp\alpha} = E_{Hp\beta} \Rightarrow P_{Hp\alpha} = P_{Hp\beta}. \quad (5)$$

Fig. 3 displays cell voltage waveforms when a modulation ratio is low. If modulation ratio $m_a \in (0.33, 0.66)$, a special thing will be considered, in which case cell voltage V_{Ha1} equals 0. The switches of cell H_{a1} cannot be triggered, so there is nearly no cell losses, however, other

2 cells cause power dissipation. In this condition, $S(1, 2) = 1$, $S(1, 3) = 1$, $\text{Rm}[S(2, 3)] < 1$, $\text{Im}[S(2, 3)] < 1$. It means that the PUD between H_{a1} and H_{a2} is high. Also, the PUD between H_{a1} and H_{a3} is high. But, the PUD between H_{a2} and H_{a3} is comparatively lower. If $m_a < 0.33$, the switches of cell H_{a2} cannot be triggered, too. So, a low modulation ratio will impede the achievement the power balance.

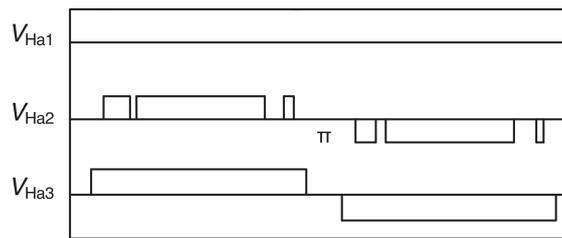


Fig. 3. a-phase H-bridge unit output voltage at low modulation ratio

Above all, conduction time difference and switching time difference among cascaded cells using the IPD strategy occur, which are the root reasons of cell loss imbalance. In addition the conduction time difference is the basic reason of output power of the cell. So, the cascaded CHB inverter can't use the IPD strategy directly, otherwise the device's lifetime will be shortened and the THD of output voltage gets worse.

3. Novel IPD-SPWM allocation strategy for CHB inverter

To avoid power imbalance among cascaded cells, some measurements should be done to improve traditional IPD strategy. As reported, trigger signal redistribution and carrier reconstruction are two main methods. However, restricting a carrier is usually more complex. The novel IPD strategy presented in this paper proposes the interchange of trigger signals in a 1/4 cycle.

Fig. 4a, b shows the sequence of the pulse set when a 7-level CHB inverter uses traditional IPD and novel IPD, respectively. The pulse set consists of all the trigger signals. Let S_{pn} be the n -th cell of the p ($p = a, b, c$) phase. So, S_{p1} is the collection of all the switch trigger signals from cell H_{p1} . Let $S_{p1} = [S_{p11} S_{p12} S_{p13} S_{p14}]$, the elements in pulse set S_{p1} are 4 switches, which can be found in Fig. 1. So, $S_{p2} = [S_{p21} S_{p22} S_{p23} S_{p24}]$ and $S_{p3} = [S_{p31} S_{p32} S_{p33} S_{p34}]$. In the shadow area of Fig. 4a, $S_{p2} = [1/0 \ 0 \ 0 \ 1/0]$ during the first half-cycle, while $S_{p2} = [0 \ 1/0 \ 1/0 \ 0]$ during the second half-cycle. In the blank area of Fig. 4a, $S_{p2} = [1 \ 0 \ 0 \ 1]$ during the first half-cycle, while $S_{p2} = [0 \ 1 \ 1 \ 0]$ during the second half-cycle. 1/0 means, the corresponding switch is turned on and off frequently; 1 represents the on state; 0 represents the off state. The pulse set displays all the switch states, which avoid illustrating the whole switches.

Fig. 4a is symmetrical. It is evident that cell losses in the first half-cycle are equal to that in the second half-cycle, but the losses of the cascaded cells are not equal to each other.

Fig. 4b shows the sequence of the pulse set when the 7-level CHB inverter uses the novel IPD strategy. From the 0 to 1/4 cycle, new pulse sets are consistent with those displayed in Fig. 4a;

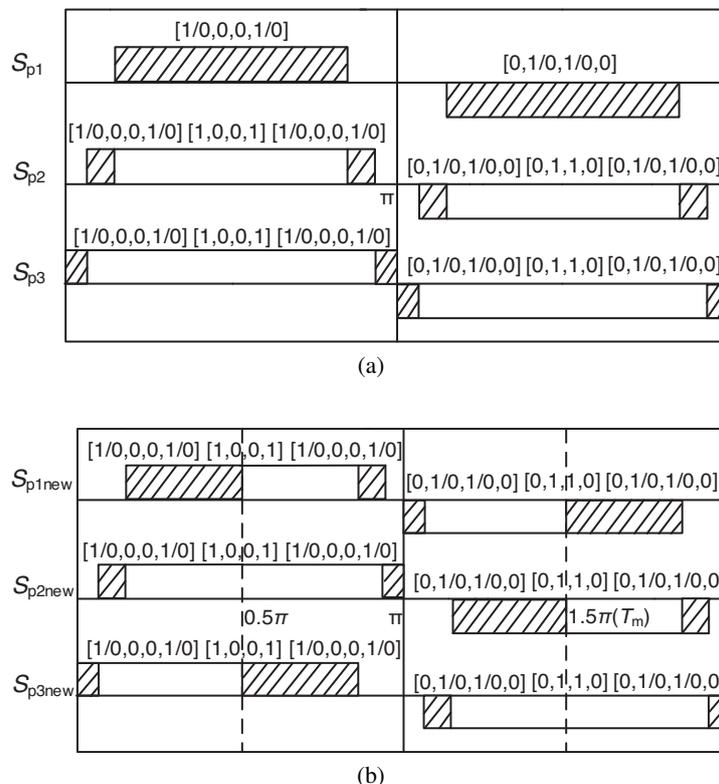


Fig. 4. Previous pulse set (a) and new pulse set (b) of CHB cells

from the 1/4 to 2/4 cycles, new pulse sets of cells in series are S_{p2} , S_{p3} , S_{p1} , they are in sequence; from the 2/4 to 3/4 cycles, new pulse sets are S_{p3} , S_{p1} , S_{p2} . The pulse allocation is completed and begins in the same way. From the 3/4 to 1 cycle, new pulse sets are consistent with that from the 0 to 1/4 cycle. During the 3/4 cycles, the device conduction time and switching times are respectively even distributed among the cascaded cells. In other words, power balance is achieved.

Table 1. Pulse allocation sequence

Cycle	H-bridge cell		
	H_{p1}	H_{p2}	H_{p3}
0~1/4	S_{p1}	S_{p2}	S_{p3}
1/4~1/2	S_{p2}	S_{p3}	S_{p1}
1/2~3/4	S_{p3}	S_{p1}	S_{p2}
3/4~1	S_{p1}	S_{p2}	S_{p3}

A new sequence of the cell pulse set is shown in Table 1 in detail. Let $T_m = 3/4$ cycles. In the author's proposed method, T_m is both a reference period and power balance period. Equations (2), (3), (4), (5) are right while substituting T_m for T . $S(\alpha, \beta) = 0$ because $t_{Hp1} = t_{Hp2} = t_{Hp3}$ and $n_{Hp1} = n_{Hp2} = n_{Hp3}$ during T_m . Hence, the power balance is achieved. In other methods [9–13], it costs one cycle or more time to achieve the power balance, while less time is needed in the author's method. This method can also be proved in another way. Considering trigger signals interchanged during T_m , Equation (4) can be rearranged as:

$$\begin{cases} E_{Hp1} = E(S_{p1}) + E(S_{p2}) + E(S_{p3}) \\ E_{Hp2} = E(S_{p2}) + E(S_{p3}) + E(S_{p1}) \\ E_{Hp3} = E(S_{p3}) + E(S_{p1}) + E(S_{p2}) \end{cases} \quad (6)$$

In Table 1 we can see that the devices in H_{p1} are triggered by the pulse sets, S_{p1} , S_{p2} , S_{p3} , which can cause losses $E(S_{p1})$, $E(S_{p2})$, $E(S_{p3})$ in sequence. Other analysis about H_{p2} and H_{p3} are analogous. Although $E(S_{p1}) \neq E(S_{p2}) \neq E(S_{p3})$, the formula $E_{Hp1} = E_{Hp2} = E_{Hp3}$ must hold. Therefore, the novel IPD strategy proposed in this paper is correct.

4. Comparison of novel IPD and other control strategy

Given the above, a sequence of cell voltage is consistent with its corresponding sequence of a cell pulse set. A new cell voltage sequence is shown in Table 2, which is similar to Table 1.

Table 2. New cell voltage sequence

Cycle	H-bridge cell voltage		
	V_{Hp1new}	V_{Hp2new}	V_{Hp3new}
0~1/4	V_{Hp1}	V_{Hp2}	V_{Hp3}
1/4~1/2	V_{Hp2}	V_{Hp3}	V_{Hp1}
1/2~3/4	V_{Hp3}	V_{Hp1}	V_{Hp2}
3/4~1	V_{Hp1}	V_{Hp2}	V_{Hp3}

V_{Hp1new} , V_{Hp2new} , V_{Hp3new} are the cell voltages when the 7-level CHB inverter uses the novel IPD. The cell voltage is interchanged per 1/4 cycle.

The new phase voltage function is expressed as:

$$V_{Pnew} = V_{Hp1new} + V_{Hp2new} + V_{Hp3new} \quad (7)$$

Although the cell voltage is interchanged per 1/4 cycle, new phase voltage V_{Pnew} is still the sum of 3 cell voltages. Compared with corresponding phase voltage when a CHB inverter uses traditional IPD, V_{Pnew} is not changed. Line voltage is also not changed, hence, the line voltage remains in low distortion.

According to the characteristics of SPWM, the dominant harmonics in the line voltage appear as sidebands around carrier frequency ω_c , which influences filter design seriously [16]. According to paper [17], a calculation formula for evaluating harmonic content around carrier frequency is shown as:

$$\left\{ \begin{array}{l} H_{\text{IPD_aN}} = \frac{\sqrt{\sum_{j=1}^{10} B_{p1}^2(1, j)}}{nm_a E}, \quad H_{\text{IPD_ab}} = \frac{\sqrt{\sum_{j=1}^{10} B_{11}^2(1, j)}}{\sqrt{3}nm_a E} \\ H_{\text{CPS_aN}} = \frac{\sqrt{\sum_{j=1}^{10} B_{p2}^2(1, j)}}{nm_a E}, \quad H_{\text{CPS_ab}} = \frac{\sqrt{\sum_{j=1}^{10} B_{12}^2(1, j)}}{\sqrt{3}nm_a E} \end{array} \right. \quad (8)$$

where, n is the number of H-bridge cells in each phase. Let $n = 3$ in 7-level CHB inverters.

$$B_{11}(1, j) = 2 \sin(2j\pi/3) B_{p1}(1, j),$$

$$B_{12}(1, j) = 2 \sin[(2j-1)\pi/3] B_{p2}(1, j),$$

$$B_{p1}(1, j) = \sum_{k=0}^{\infty} \left\{ A \left\{ -B \sin(B\pi/2) - C \sin(C\pi/2) + \right. \right. \\ \left. \left. + 2 \sum_{h=0}^{n-1} \left\{ \cos(h\pi) \sin \left\{ (B+C) \arccos [h/(nm_a)] \right\} \right\} \right\} \right\},$$

$$A = 4E(-1)^k J_{2k+1}[\pi nm_a]/(\pi^2), \quad B = (2j-2k-1)^{-1}, \quad C = (2j+2k+1)^{-1},$$

$$B_{p2}(1, j) = 2E J_{(2j-1)}(n\pi m_a)/(\pi).$$

J is the Bessel function.

Fig. 5 shows an output voltage harmonic of IPD and CPS strategy when $m_a \in (0, 1)$. Fig. 5a displays a phase voltage harmonic changing curve. The changing curve of the IPD and that of CPS share almost the same value and shape. In Fig. 5b, less harmonic content exists in line voltage, when the CHB inverter uses a traditional IPD strategy. A new line voltage is not changed compared with the traditional IPD. That is to say, the novel IPD inherits the advantage of a less line voltage harmonic.

As reported, trigger signal redistribution and carrier reconstruction are two main methods to achieve power balance [14–15].

According to switch redundancy and dc source redundancy in cascaded inverter, Paper [10] presents a method to balance the usage rate of a switch and dc source. That is randomly selecting one satisfying constraint switch state combination to achieve required level voltage per switching cycle. Efficiency of this method depends on time length of achieving power balance, but it is difficult to evaluate the time without simulation. Simulation has been done to generate random switch state combination per switching cycle. After 1000 switching cycles, the usage rate of each cell is going to be the same. According to the characteristic of SPWM, a switching cycle is equal to a carrier wave period. If carrier wave frequency equals 10 KHz and modulation wave

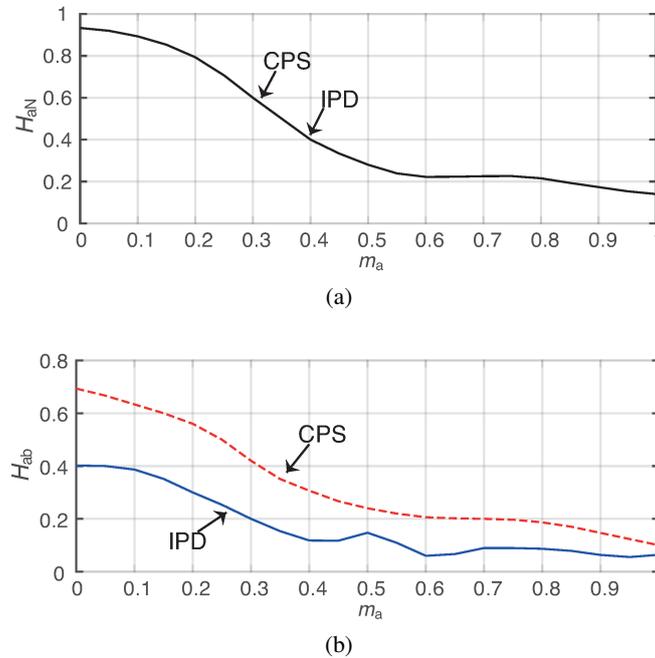


Fig. 5. Waveforms of phase voltage harmonic and line voltage harmonic in IPD and CPS strategy: phase voltage harmonic H_{aN} versus m_a (a); line voltage harmonic versus m_a (b)

equals 50 Hz, there are more than 200 groups of repeatable switch state combination generated within 0.02 s. So, it costs at least 50 power frequency periods to achieve power balance, which is not acceptable for a machine changing working mode frequently, especially in high power applications.

Paper [17] proposes a new method to achieve power balance by changing partially mutual position of carrier wave of IPD and carrier wave of CPS. This method achieves power balance within a cycle and possesses the advantage of IPD. But, some formula deduction should be done to re-analyze voltage harmonic.

Above all, novel IPD proposed in this paper is a simple way to implement power balance and it cost less time.

5. Simulation and experiment results

5.1. Simulation results

In order to verify the novel IPD strategy, a simulation testing platform is built by Matlab. All simulation results are in the condition of modulation frequency equaling 50 Hz and carrier frequency equaling 10 KHz. Fig. 6 shows cell voltage waveforms of novel IPD when a modulation ratio is $m_a = 0.99$. Fig. 7 shows phase voltage and line voltage waveforms when $m_a = 0.99$.

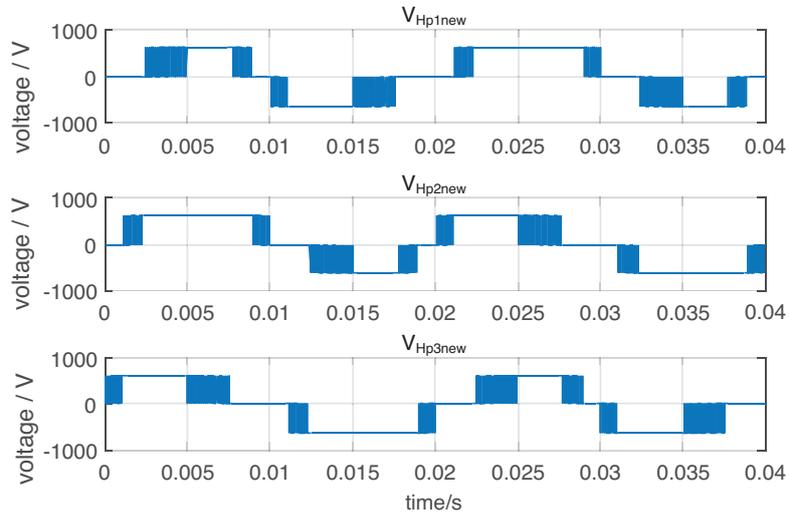


Fig. 6. Simulated waveforms of cell voltages in novel IPD when $m_a = 0.99$

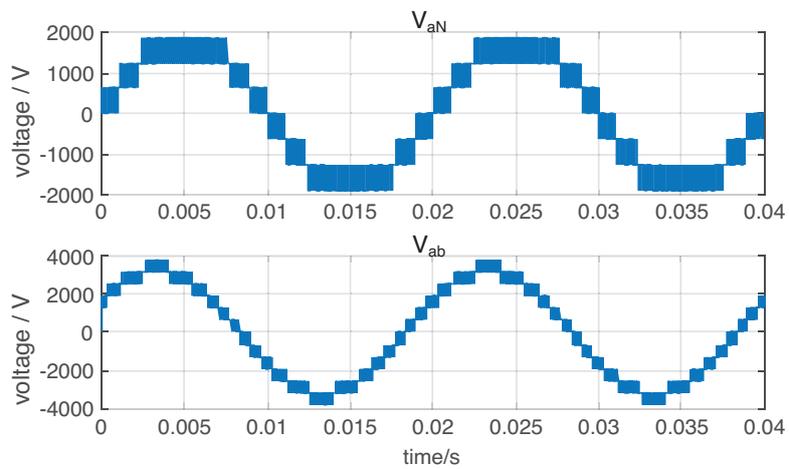


Fig. 7. Simulated waveforms of V_{aN} and V_{ab} in novel IPD when $m_a = 0.99$

Fig. 8 shows simulated results for traditional IPD and novel IPD when $m_a = 0.6$. Fig. 8a and b shows cell voltage waveforms of traditional IPD and the novel IPD method.

Some conclusion can be obtained through the simulated result. Cell voltage waveforms are interchanged per 1/4 cycle, which synthesizes expected phase voltage and line voltage waveforms. It achieves power balance with 3/4 cycles. In Fig. 8, Power unbalance degree can be calculated by using e.g. (2). $S(1, 2) = 1, S(1, 3) = 1$ when $m_a = 0.6$, because cell H_{p1} has no voltage output. It means cell losses are undistributed seriously. The novel IPD solves the problem by interchanging

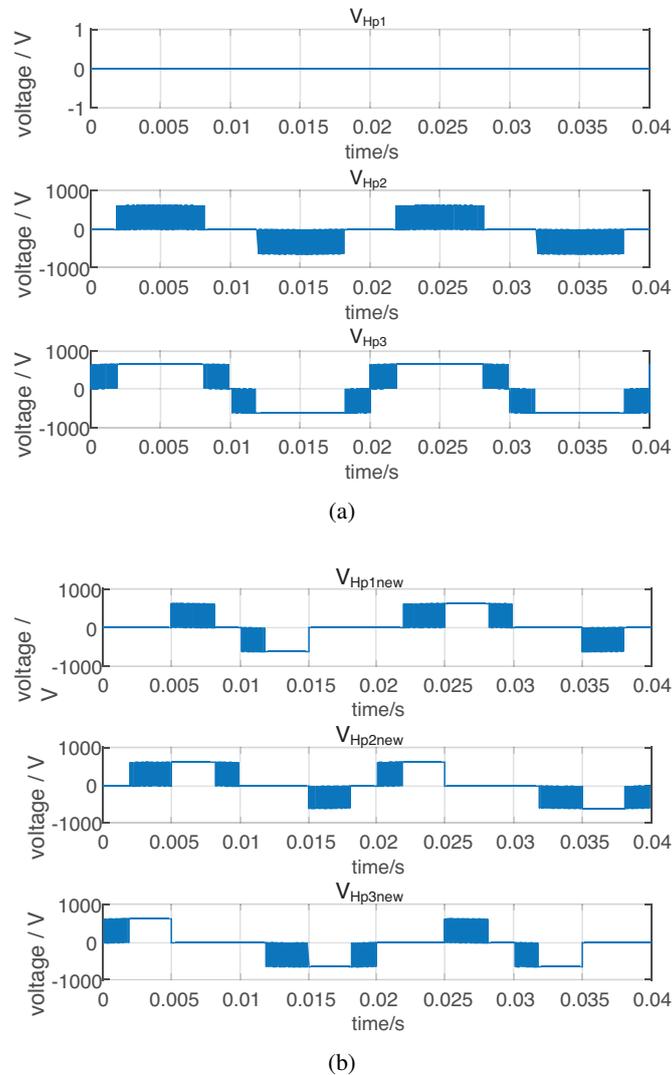


Fig. 8. Simulated waveforms of cell voltage when $m_a = 0.6$ in traditional IPD (a), novel IPD (b)

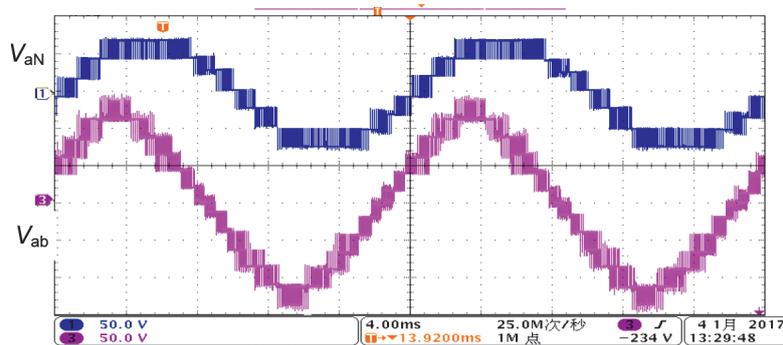
trigger signals when $m_a = 0.6$. It achieves power within 3/4 cycles, too. According to e.g. (2) and (6), $S(1, 2) = S(1, 3) = S(2, 3) = 0$ and $E_{Hp1} = E_{Hp2} = E_{Hp3}$ after using the novel IPD.

5.2. Experimental results

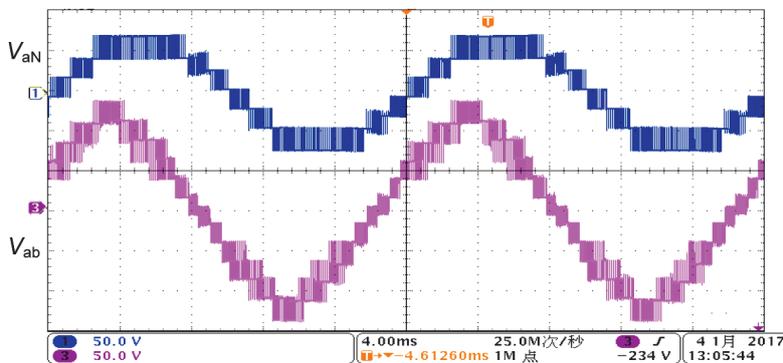
In order to verify the above theoretical analysis, a prototype of a 7-level CHB inverter was developed, and controlled via 3 DSPs (TMS320F2812) running online. Every CHB cell includes 4 IGBTs (IKP15N60T). A DC source $E = 24$ V is designed for each H-bridge cell. Load R is

assumed as 200Ω . All experimental results are in the condition of modulation frequency equaling 50 Hz and carrier frequency equaling 10 KHz.

Fig. 9 shows the experimental results for phase voltage and line voltage of the traditional IPD and novel IPD. In Fig. 9a, waveforms of phase voltage V_a and line voltage V_{ab} are consistent with their corresponding waveforms in Fig. 9b. It means the phase voltage and line voltage are not changed when a cascaded CHB inverter uses the novel IPD, which inherits the advantage of the traditional IPD.



(a)

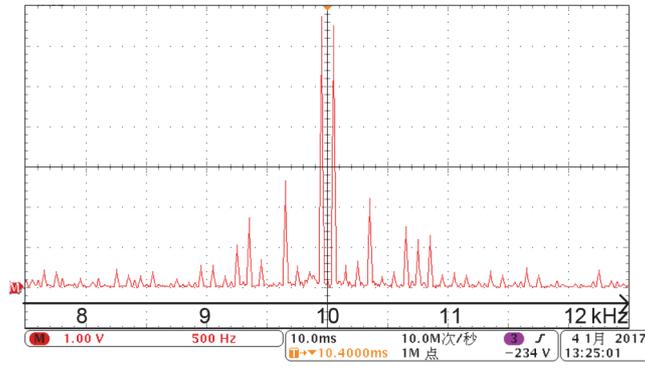


(b)

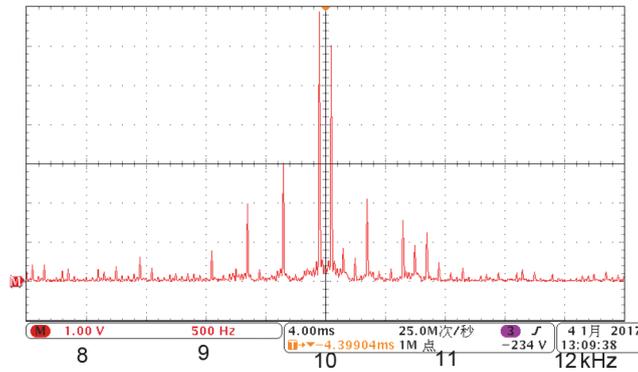
Fig. 9. Waveforms of phase voltage and line voltage in novel IPD (a), traditional IPD (b)

The spectra of V_{ab} are shown in Fig. 10a and b, where the waveforms in the novel IPD method are similar to that in the CPS method.

Fig. 11 shows waveforms of cell voltage during a cycle, which is similar to Fig. 4. In Fig. 11a, waveforms of cell voltage are interchanged per 1/4 cycle. For example, V_{Ha2new} is consistent with V_{Ha2} in the first 1/4 cycle and with V_{Ha3} in the second 1/4 cycle and with V_{Ha1} in the third 1/4 cycle. It achieves power balance within T_m .



(a)



(b)

Fig. 10. Spectrogram of line voltage V_{ab} in novel IPD (a), traditional IPD (b)

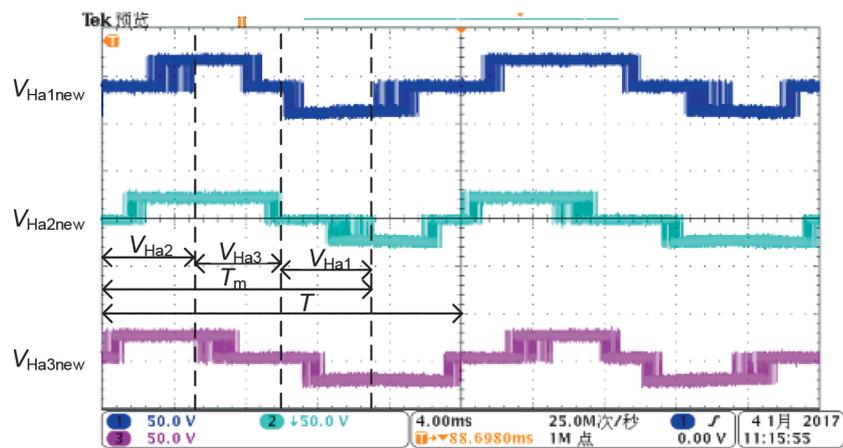


Fig. 11(a)

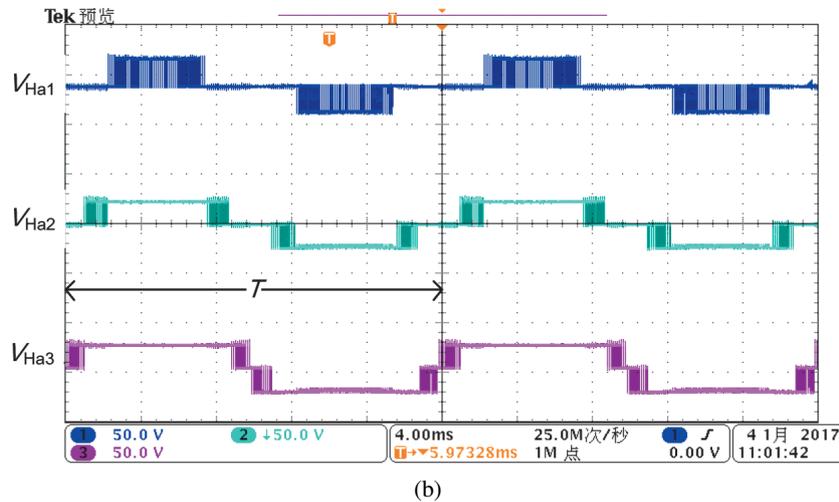


Fig. 11. Waveforms of cell voltages in a phase with novel IPD (a), traditional IPD (b)

The output power value of a phase cells are measured and found to be almost the same. It further verifies the validity of the analysis and effectiveness of the proposed novel IPD strategy.

6. Conclusions

A novel IPD-SPWM allocation strategy is presented. The working principle of this method is analyzed in detail. The proposed method overcomes the shortcoming of a traditional IPD strategy, and it inherits the line voltage characteristic of the traditional IPD strategy. Compared with other power balance methods, the proposed method achieves power within less time, which only costs 3/4 cycles. The correctness of the proposed inverter is verified through simulation and experimental results

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References

- [1] Zhang Y., Sun L., Zhao K., Wang Y., *Optimized control of modulation strategy for hybrid H-bridge cascaded multilevel inverter*, Electric Power Automation Equipment, vol. 30, no. 5, pp. 63–66 (2015).
- [2] Wang Z., *The research on multilevel diode-clamped inverter capacitor voltage balancing SVM strategy and its application*, Master Thesis, Hunan University, Changsha (2014).

- [3] Mittal N., Singh B., Singh S., Dixit R., Kumar D., *Multilevel inverters: A literature survey on topologies and control strategies*, IEEE Power, Control and Embedded Systems (ICPCES), Allahabad, India, pp. 1–11 (2012).
- [4] Wang S., Zhao J., Yao X., Sun Y., *Power balanced controlling of cascaded inverter for grid-connected photovoltaic systems under unequal irradiance conditions*, Transactions of China Electrotechnical Society, vol. 28, no. 12, pp. 251–261 (2013).
- [5] Peng H., Deng Y., Wang Y., Wang K., He X., Zhao R., *Research about the Model and Strady-state Performance for Modular Multilevel Converter*, Transactions of China Electrotechnical Society, vol. 30, no. 12, pp. 251–261 (2015).
- [6] Peng F.Z., McKeever J.W., Adams D.J., *A power line conditioner using cascade multilevel inverters for distribution systems*, IEEE Industry Applications Conference, New Orleans, USA, pp. 1316–1321 (1997).
- [7] Sun C., Zhang J., Ji Z., *Control strategy of DC voltage balance and power equilibrium for grid-connected cascaded H-bridge converters*, Electric Power Automation Equipment, vol. 34, no. 1, pp. 55–60 (2014).
- [8] Hao T., Wang G., Zeng J., Dutta S., *Voltage and power balance control for a cascaded multilevel solid state transformer*, IEEE Applied Power Electronics Conference and Exposition, Palm Springs, USA, pp. 761–767 (2010).
- [9] Wang X., Zhang X., Ruan X., *Optimal Spwm control Strategy and its power balance scheme for cascaded multilevel inverters*, Transactions of China Electrotechnical Society, vol. 24, no. 5, pp. 92–99 (2009).
- [10] Chan Q., Pan M., Li S., Hu K., *Random pwm distribution of cascaded inverter*, Proceedings of the CSEE, vol. 24, no. 2, pp. 157–161 (2004).
- [11] Wang H, Zhao R., Deng Y., He X., *Novel carrier-based PWM methods for multilevel inverter*, IEEE Industrial Electronics Society, Roanoke, USA, pp. 2777–2782 (2003).
- [12] Wang K., Feng L., Li G., *A novel carrier-based disposition PWM method with voltage balance for flying-capacitor multilevel inverter*, Power System Protection and Control, vol. 42, no. 14, pp. 8–13 (2014).
- [13] Xu J., Wang K., Zhai D, Feng L., Li G., *A novel carrier-based disposition pwm method with voltage balance for flying capacitor multilevel inverter*, Power System Protection and Control, vol. 43, no. 12, pp. 134–139 (2015).
- [14] Chan Q., Li Y., Pan M., *A Review on Cascaded Inverter*, Transactions of China Electrotechnical Society, vol. 19, no. 2, pp. 1–9 (2004).
- [15] Geng J., *Research on cascade multilevel inverter and control strategy*, Master These, Beijing Jiaotong University, Beijing (2015).
- [16] McGrath B.P., Holmes D.G., *A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters*, IEEE Annual Power Electronics Specialists Conference, Galway, Ireland, pp. 674–679 (2000).