

Positive output elementary Luo converter for fixed-frequency ZVS operation

S.J.V. BRIGHT^{1*}, S. RAMKUMAR², and H. ANAND³

¹Department of EEE, Maria College of Engineering & Technology, Attoor, 629177, Tamil Nadu, India

²Department of EEE, Sri Krishna College of Engineering & Technology, Coimbatore, 641008, Tamil Nadu, India

³Department of EEE, SSN College of Engineering, Kalavakkam, Chennai, 603110, Tamil Nadu, India

Abstract. Luo converter is one amid the developed DC-DC converters offering higher voltage gain. Soft-switching techniques, like zero-voltage switching (ZVS), repress switching losses, and hence the system efficiency and the life of the power semiconductor switches are improved. Incorporation of soft switching in fixed-frequency operation of the Luo converters may persuade them in the regulated power supply applications. The existing variable switching frequency solution suffers from a number of problems viz. complexity in filter designing, more electromagnetic interference (EMI), etc. This paper proposes a positive output elementary Luo converter (POELC) involving ZVS with the wherewithal of working in fixed frequency. A comprehensive discussion on the proposed circuit topology is detailed with both simulation and experimental studies. Systematic descriptions of basic POELC, variable-frequency ZVS-POELC, and fixed-frequency ZVS-POELC make an impact on the understanding of related concepts by the researchers in this field.

Key words: fixed-frequency ZVS, positive output elementary Luo converter (POELC), zero-voltage switching-pulse width modulation (ZVS-PWM).

1. Introduction

DC-DC converters are now an indistinguishable module in applications ranging from low power actuators to high power drives [1]. The applications of DC-DC converters include laptops, mobile gadgets, switched-mode power supplies (SMPS), auxiliary power supplies to various systems, drives, etc. F. L. Luo has developed low ripple, yet high gain converters in the 1970s. Luo converter (LC) offers less voltage ripple in simple configuration [2, 3]. The basic LC has a high voltage gain and high power density [4]. Its variants use the voltage lift technique (VLT), super-lift technique (SLT) and ultra-lift technique (ULT) for improving the voltage gain. Furthermore, both VLT and SLT have positive and negative output subclasses. The positive and negative circuits of VLT can be subdivided into elementary, self-lift, re-lift and multiple-lift circuits [2]. The re-lift circuit of main series using SLT is derived from the elementary circuit by adding one inductance, three diodes, and two capacitors. The devious triple-lift circuit of main series using SLT is derived from re-lifts circuit by adding one inductance, three diodes, and two capacitors [3]. The additional series using SLT is derived from main series by adding the two diodes and two capacitors only. Each type of LC has one or more ‘pumping circuits’ and a filter circuit.

The power switch of each LC is controlled through a pulse-width modulated (PWM) signal with a switching time period (T) and a duty cycle (d). The energy is transferred from the source to the load through the pumping circuit during the ON

state (dT). During the OFF state ((1-d)T), the energy transfer is blocked. The control methodology for these converters is PWM. The conventional PWM converters are also called ‘hard-switched converters’.

At high switching frequencies, these hard-switched converters suffer from high switching stress, high switching power losses, reduced reliability and electromagnetic interference (EMI) [5]. To overcome these difficulties, soft-switching techniques like zero-voltage switching (ZVS) have been introduced in LCs [6–8]. The ZVS technique expunges the large capacitance of the main switch through resonant switching, which minimizes the losses, as well as reduces the ringing in waveforms [9]. The soft-switching technique in LC has helped in escalating the switching frequency, hence casting a compact converter of a higher power density than that of the PWM converters [3]. ZVS was easier in high-current applications, and a reasonably low EMI has been observed [3]. Even though the frequency of switching is reasonably increased, the voltage stress across the main switch is also increased. In ZVS, the voltage across the main switch can reach eleven times the input voltage [9]. The voltage regulation in ZVS-LC is more liberally achieved by variable frequency operation [6]. The variable frequency operation results in high voltage stress on switches (hence the minimal reliability of power switches) and complexity of filter design.

This paper proposes a modified topology to support the fixed-frequency ZVS in overcoming the abovementioned issues of the positive output elementary Luo converter (POELC). The main idea of the modified topology is adding an auxiliary switch across the resonant inductance, which delays the immediate resonant cycle until its turned OFF. Using variable pulse

*e-mail: shibubright@gmail.com

width generator logic, ON time is controlled in constant frequency (CF). The MATLAB-Simulink simulation validates the functionality of the POELC topology and ZVS-PWM strategy. Further corroboration is found using field programmable gate array (FPGA) accorded experimental prototype.

2. Luo converter and soft switching

By incorporating certain types of resonant network into a PWM switched converter topology, numerous resonant converters can be formed, through either the ZVS or a zero-current switching (ZCS) condition for the switches [10]. This improvement significantly reduces switching losses and enables the converter to operate at a higher switching frequency.

2.1. Positive output elementary Luo converter. Basic LC has a positive output, as well as negative output configurations. This is the work that POELC is considered with, which is drawn in Fig. 1. It consists of a positive Luo pump circuit, a low-pass filter (L_2 & C_o), and a load circuit. The pump inductance (L_1) transfers the stored energy to capacitor (C) during switch-off, and then the stored energy on C is delivered to the load (R) during the ON state. C acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductance (L_1). Assuming that C is sufficiently large, the variation of the voltage across C from its average value V_o can be neglected in steady state.

There are two modes of operation in POELC. In mode 1 (Fig. 2), when switch (S) is turned ON, L_1 and L_2 absorb the en-

ergy from the source. The current flowing during the switch-on is given as follows:

$$i_s = i_{L1} + i_{L2}, \tag{1}$$

where i_s is the source current, i_{L1} and i_{L2} are the current flowing through inductances L_1 and L_2 respectively.

In mode 2, when S is turned off, the source current is zero and i_{L1} freewheels through the diode (D) and charging the capacitor (C). The current i_{L2} maintains the same flow direction. Equivalent circuit for mode 2 is shown in Fig. 3.

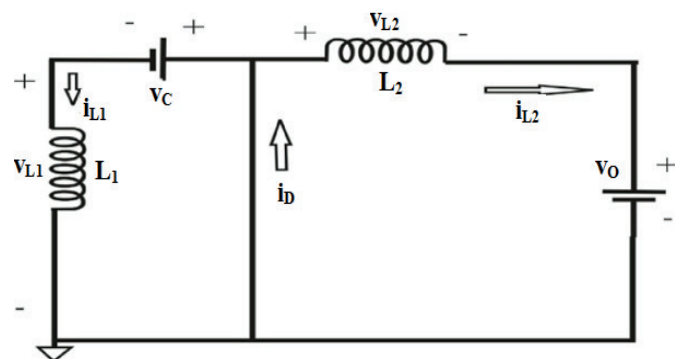


Fig. 3. Mode 2 of POELC

Under steady state operation, it is assumed that the charge in C remains unfazed. Output voltage is derived as

$$V_o = \left(\frac{d}{1-d}\right)V_{in}. \tag{2}$$

2.2. Zero-voltage switching in POELC. The voltage across the main switch (S) is resonated and descended to zero voltage (zero crossing) for achieving ZVS operation. Various possible soft-switching topologies have been archived [11–14]. By adding an anti-parallel diode (D_1), resonant capacitor (C_r) and resonant inductance (L_r) (this combination forms a tank circuit), half-wave ZVS can be achieved in POELC. Schematic for ZVS-POELC is shown in Fig. 4.

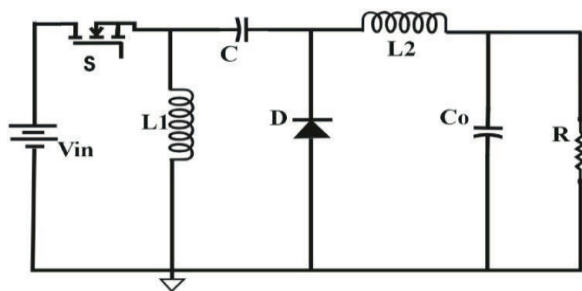


Fig. 1. Circuit diagram of POELC

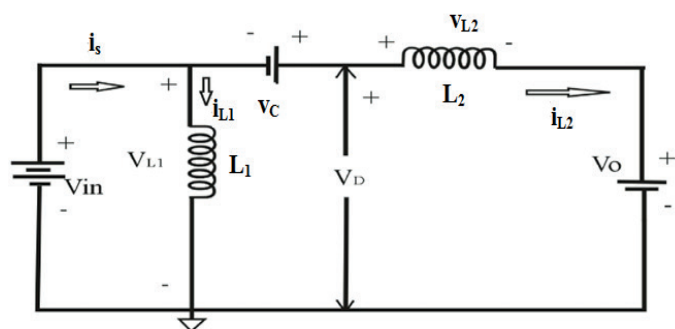


Fig. 2. Mode 1 of POELC

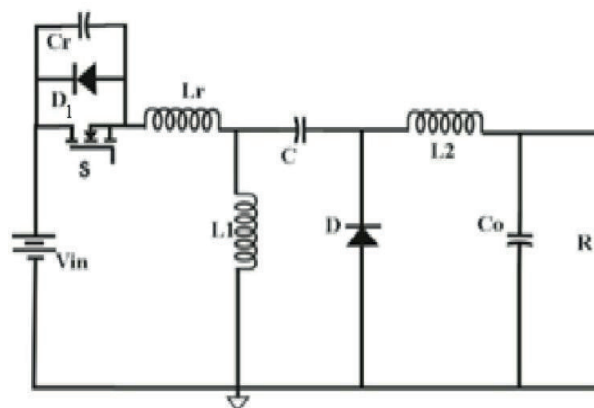


Fig. 4. Circuit diagram of ZVS-POELC

The ZVS operation of POELC has four modes of operation [6]. In mode 1, the switch (S) is in the OFF state and input current causes an increase in capacitor voltage to the magnitude equal to the input voltage as shown in Fig. 5.

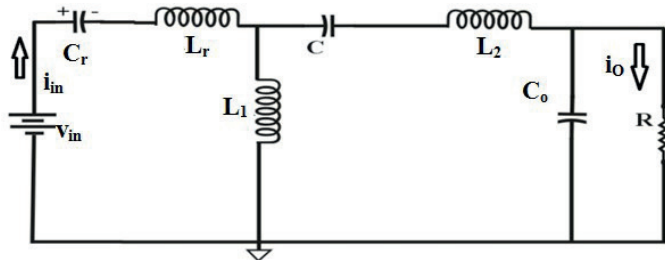


Fig. 5. Mode 1 of ZVS-POELC

In mode 2, since diode (D) becomes forward-biased, resonant inductance current decreases. The capacitor (C) is charged through D. Series resonance happens between L_r and C_r , and the corresponding equivalent circuit is shown in Fig. 6.

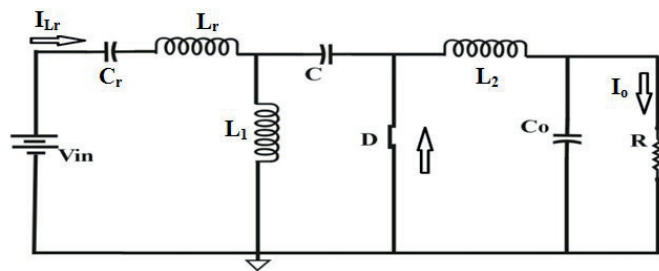


Fig. 6. Mode 2 of ZVS-POELC

In mode 3, when the resonant capacitor voltage reaches zero crossing, the switch is turned ON, hence achieving the ZVS. The equivalent circuit is shown in Fig. 7.

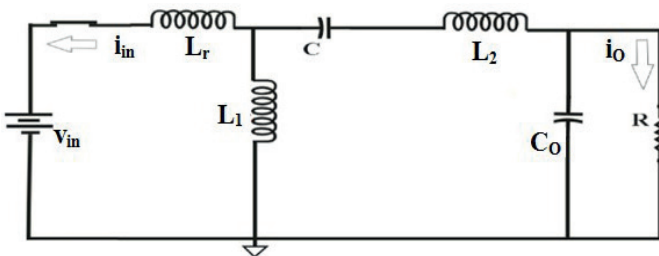


Fig. 7. Mode 3 of ZVS-POELC

In mode 4, the switch remains in the ON condition and input current flows in the positive direction. Inductor L_1 is pumped. This mode of operation lingers until S is turned OFF. The equivalent circuit is shown in Fig. 8.

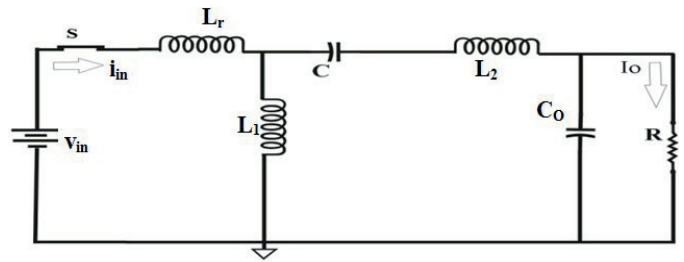


Fig. 8. Mode 4 of ZVS-POELC

The cycle reaffirms and soft switching is achieved in POELC. In ZVS, the resonant peak voltage across the switch can be three to five times that of the rating used in hard switching. It is worth noting that the discussed scheme results in variable frequency operation [15–18]. The voltage stress can be minimized by using an effective ZVS-PWM technique. The theoretical waveforms of the switching described above are presented in Fig. 9.

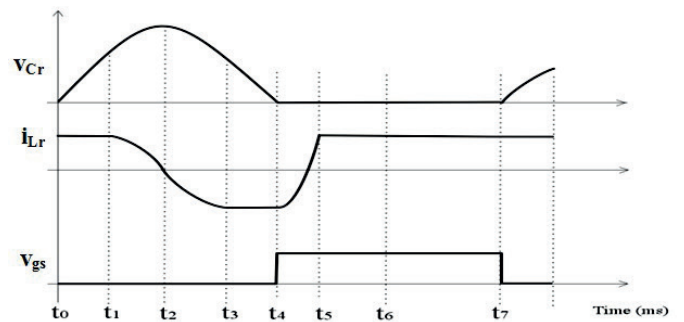


Fig. 9. Theoretical waveforms of ZVS-POELC

3. Proposed circuit

The proposed circuit consists of the POELC, a ZVS resonant tank circuit attached with main switch (S), and an auxiliary switch (S_1), connected across the resonant inductance (to operate the POELC in fixed frequency), as shown in Fig. 10.

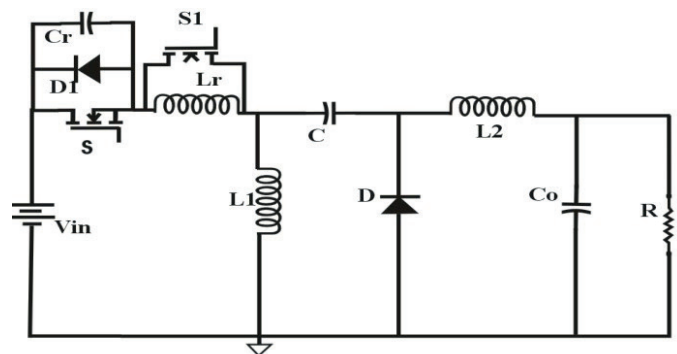


Fig. 10. Circuit diagram of ZVS-PWM POELC

The main objective is to achieve the fixed frequency operation through topology supported ZVS-PWM scheme.

The modes of operations of the proposed circuit are explained for a complete working cycle (t_0-t_7). The inverse of the duration of a cycle gives the switching frequency of the converter. Theoretical waveforms for different modes are given in Fig. 11.

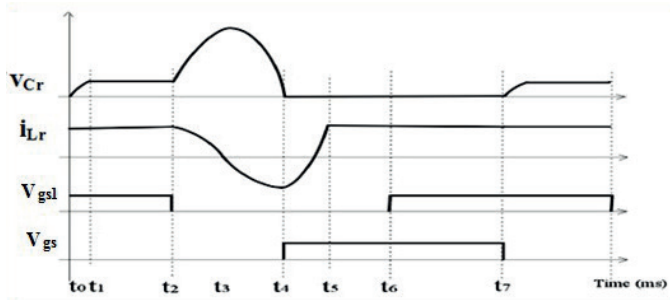


Fig. 11. Theoretical waveforms of ZVS-PWM POELC

In mode 1, the main switch (S) is in the OFF state and the resonant capacitor is charged from t_0 time to t_1 . The auxiliary switch (S_1) is in the ON state and the resonant inductance current is maintained. The equivalent circuit is diagrammed Fig. 12.

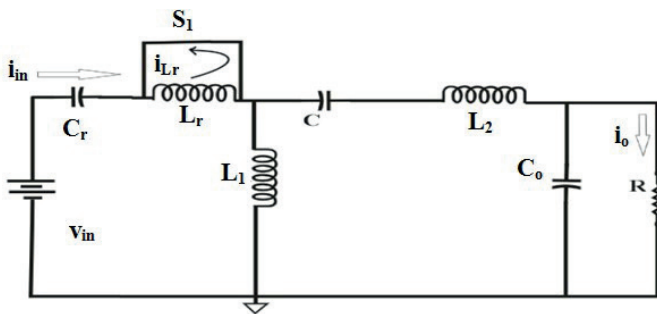


Fig. 12. Mode 1 of ZVS-PWM POELC

In mode 2, resonance is initiated starting from t_2-t_4 . At t_3 , when the resonant capacitor voltage is maximum, the resonant inductance current reaches zero. At t_4 , the resonant capacitor voltage is zero, and the diode (D) starts to conduct. The equivalent circuit is sketched in Fig. 13.

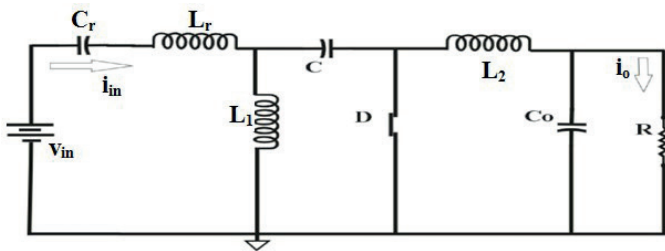


Fig. 13. Mode 2 of ZVS-PWM POELC

In mode 3, when the resonant capacitor voltage is zero, the main gate pulse is given, achieving ZVS. Time t_4-t_6 gives the main gate pulse duration. Resonant inductance current is increased to its maximum at time t_5 . This mode includes linear recovering interval and pumping. The equivalent circuit is pictured in Fig. 14.

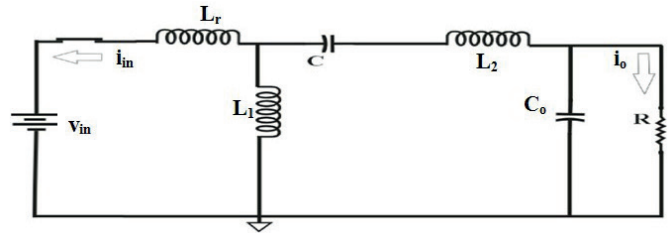


Fig. 14. Mode 3 of ZVS-PWM POELC

In mode 4 (t_6-t_7), the main gate pulse lingers in the ON state and the auxiliary gate pulse is initiated at t_6 . S_1 continues to be in the ON state for next cycle. Hence, the cycle reaffirms. Pumping continues as normal PWM converter. The equivalent circuit is depicted in Fig. 15.

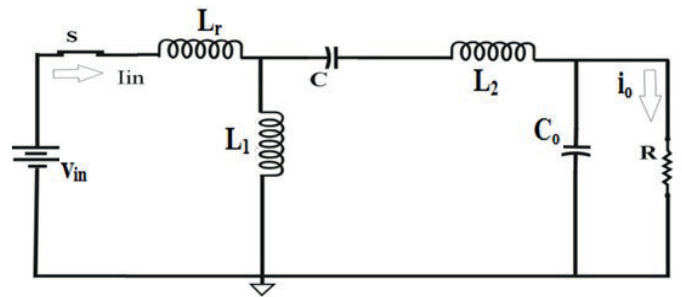


Fig. 15. Mode 4 of ZVS-PWM POELC

4. Simulation results

The POELC is designed for 10 V DC input, switching frequency of 50 kHz, and other strictures viz. $L_r = 10 \mu\text{H}$, $L_1 = 11 \text{ mH}$, $L_2 = 1 \text{ mH}$, $C = C_0 = 20 \mu\text{F}$, $C_r = 0.1 \mu\text{F}$, and load resistance $R = 10 \Omega$ [19–20]. The basic POELC, ZVS-POELC (variable frequency) and ZVS-PWM POELC are simulated for similar specifications in MATLAB-Simulink environment (r2010a) with other parameter configurations viz. ode solver-ode23tb (stiff/TR-BDF2), variable step type of simulation, maximum step size of $1e-5$, auto minimum step size, and initial step size $1e-6$. Waveforms showing the voltage across the resonant capacitor, current in resonant inductance, and the gate pulse (V_{gs}) of ZVS-POELC (variable frequency switching) are indicated in Fig. 16. The output voltage of ZVS-PWM POELC for duty cycle (d) of 50% and the input voltages are shown in

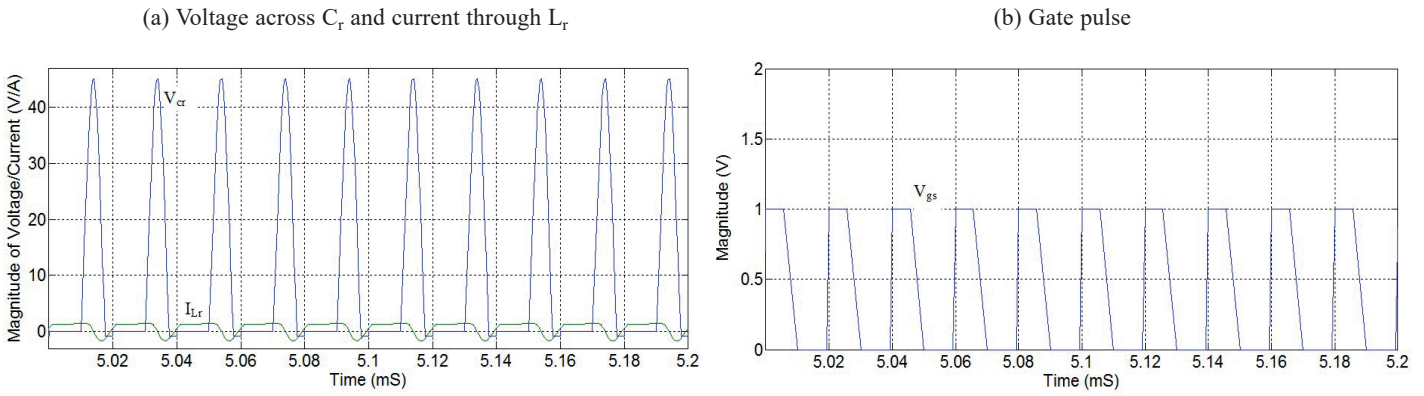


Fig. 16. Waveforms – ZVS-POELC

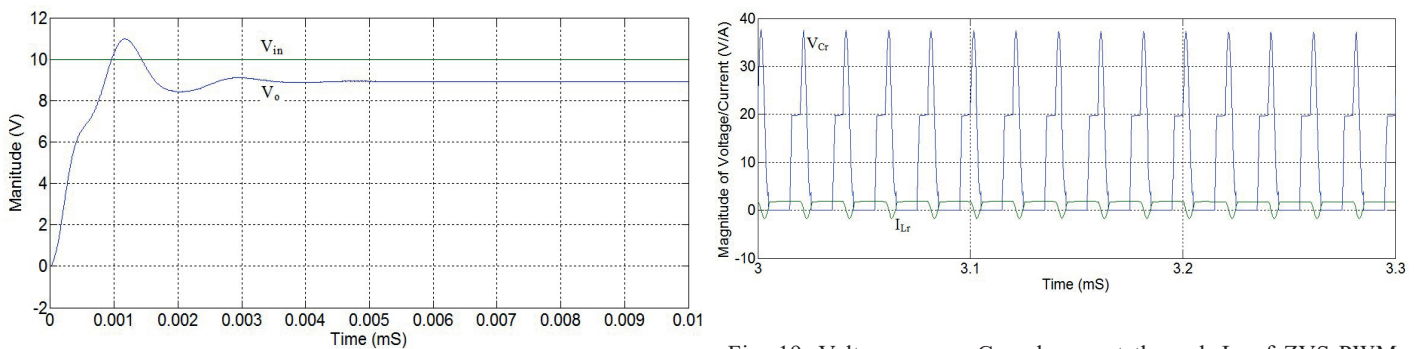


Fig. 17. Output voltage and input voltage – $d = 50\%$

Fig. 19. Voltage across C_r and current through L_r of ZVS-PWM POELC for $d = 50\%$

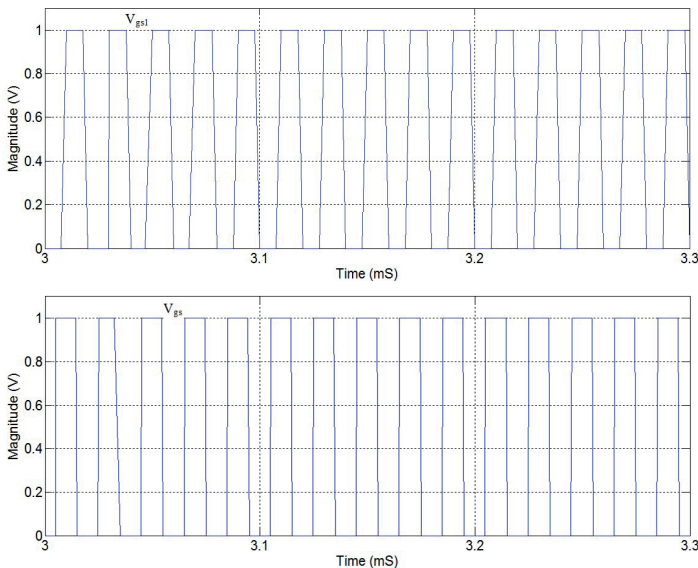


Fig. 18. Main and auxiliary gate pulses of ZVS-PWM POELC – $d = 50\%$

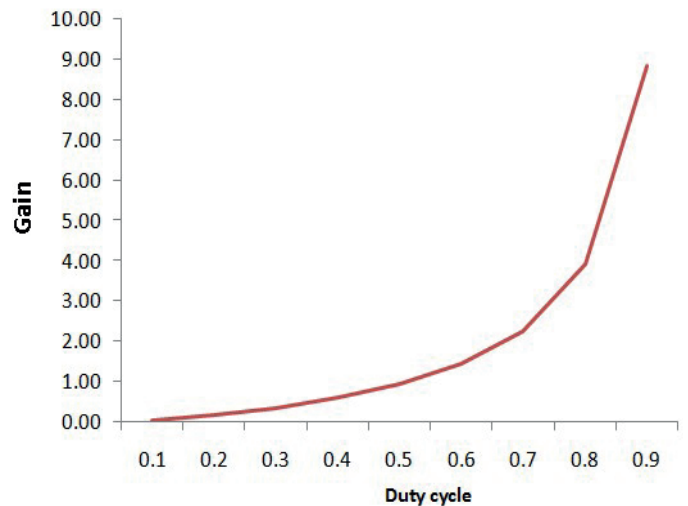


Fig. 20. Duty cycle versus voltage gain

Fig. 17. The pulses of main (V_{gs}) and auxiliary (V_{gs1}) switches of ZVS-PWM POELC are pictured in Fig. 18 for $d = 50\%$, while the key waveforms are presented in Fig. 19. The vari-

ation of voltage gain against the duty cycle is illustrated in Fig. 20. Fig. 21 shows the ripple present in output voltage at a steady state as 0.012 V.

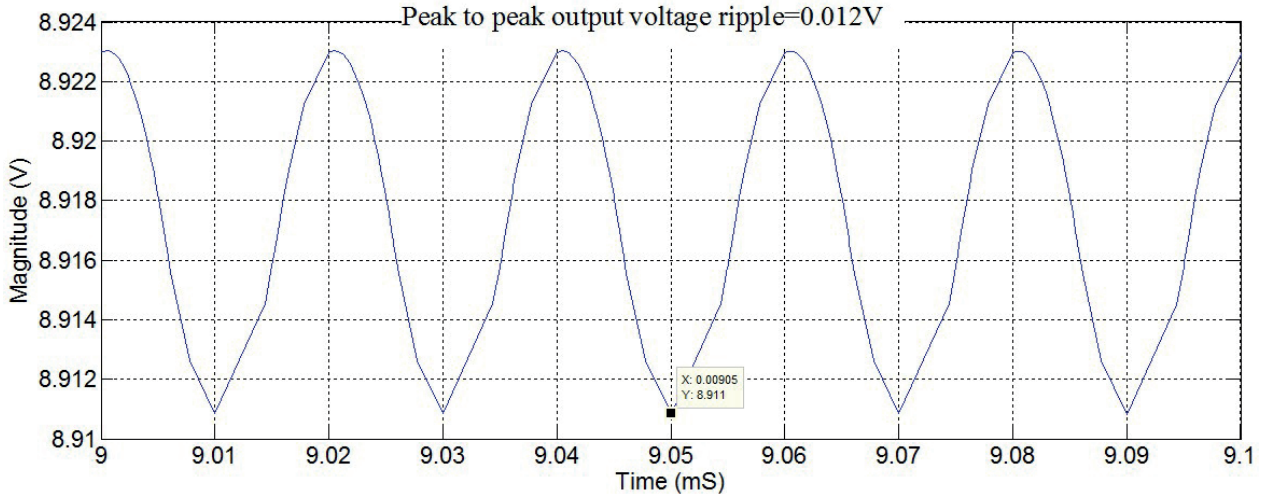


Fig. 21. Ripple in output voltage at steady state

5. Experimental corroboration

The simulation results are vindicated through an experimental exploration. A prototype ZVS-PWM POELC is developed for the specification used in the simulation study. MOSFET IRFN540 is taken as power switch, the D is FR306, while the D_1 is the integral body diode of IRFN540, capacitors $C = C_0 = 20 \mu\text{F}$, $C_r = 0.1 \mu\text{F}$ are electrolytic and plain polyester type, and the inductance is constructed in ferrite core. The complete experimental setup is detailed in Fig. 22. The proposed controllers are implemented using the very high speed integrated circuit (VHSIC) hardware description language (VHDL) [21]. The functional simulation study of the archi-

itecture is performed using the tool ModelSim 6.3. The register transfer level (RTL) confirmation and accomplishment are performed using the synthesizing tool Xilinx ISE 13.2. Then the designed architecture is configured to the SPARTAN-6 FPGA (XC6SLX45) device. The RTL schematic, device utilization and logic implementation can be verified as shown in Fig. 23, Table 1, and Fig. 24, respectively.

Figure 25 shows the developed ZVS-PWM POELC, and the representative input and output voltages are pictured in Fig. 26. The figure corroborates the similar situation in the simulation study (Fig. 17). The ripple in the output voltage is studied in Fig. 27. The ripple obtained in the simulation study is 0.012 V, while through experimentation it is 0.013 V.

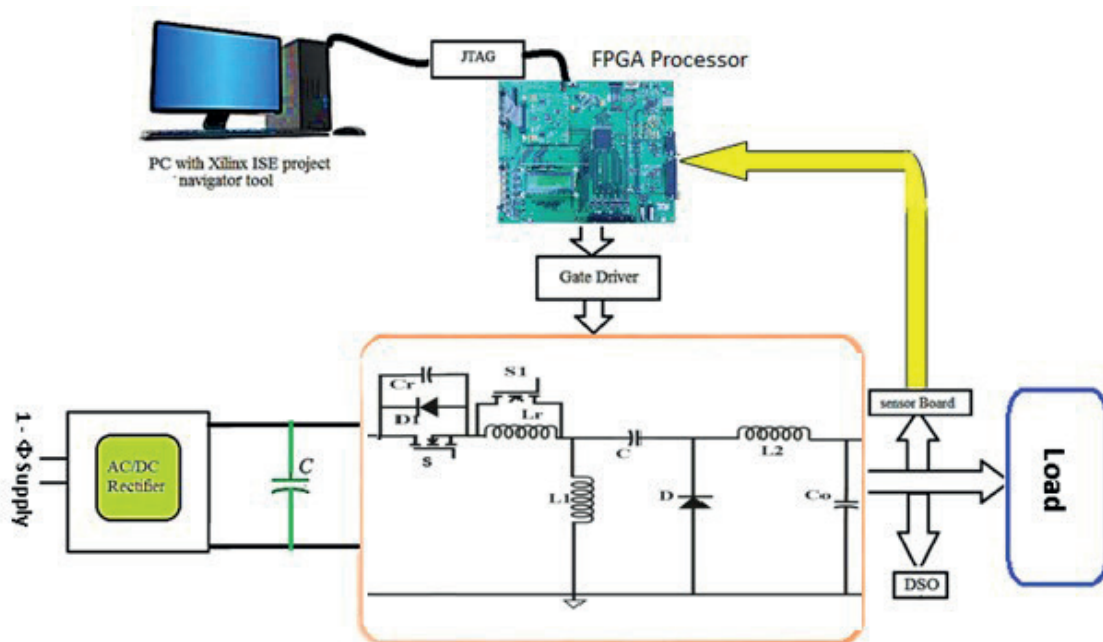


Fig. 22. Experimental setup

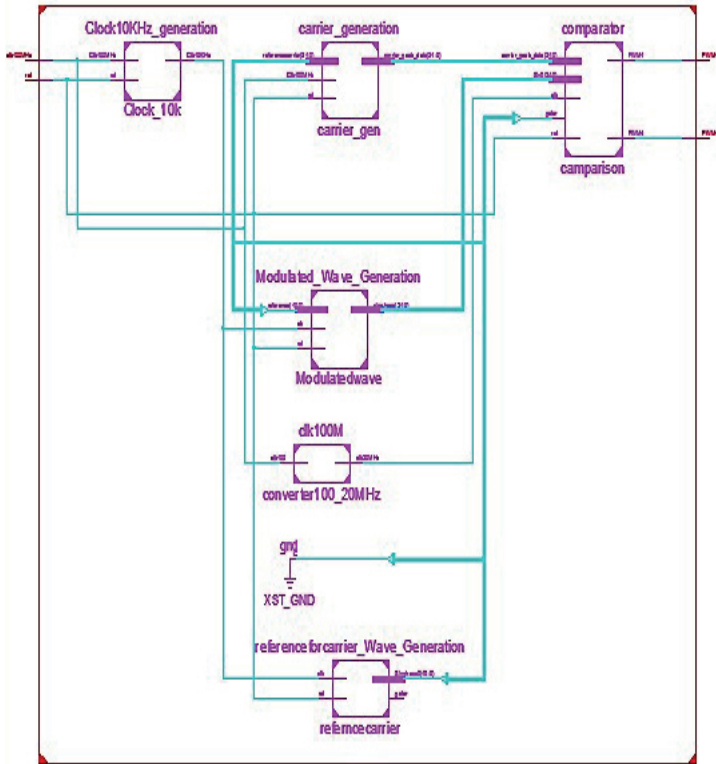


Fig. 23. RTL Diagram for RPWM 8-bit PRBS

Table 1
Device utilization summary (estimated values)

Logic utilization	Used	Available	Utilization
Number of slice registers	325	30064	1%
Number of slice LUTs	793	15032	5%
Number of fully used LUT-FF pairs	228	890	25%
Number of bonded IOBs	10	186	5%
Number of BUFG/ BUFGCTRLs	5	16	31%
Number of DSP48A1s	3	38	7%

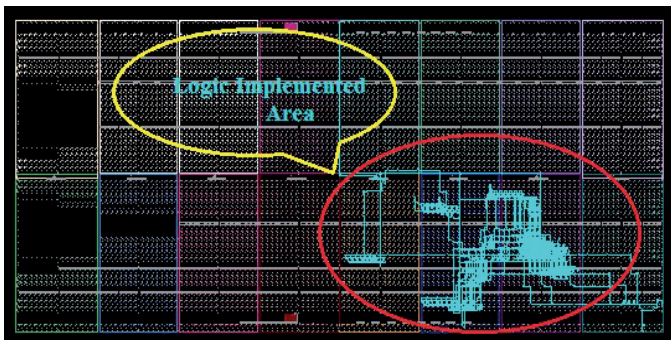


Fig. 24. Logic implemented area for the architecture

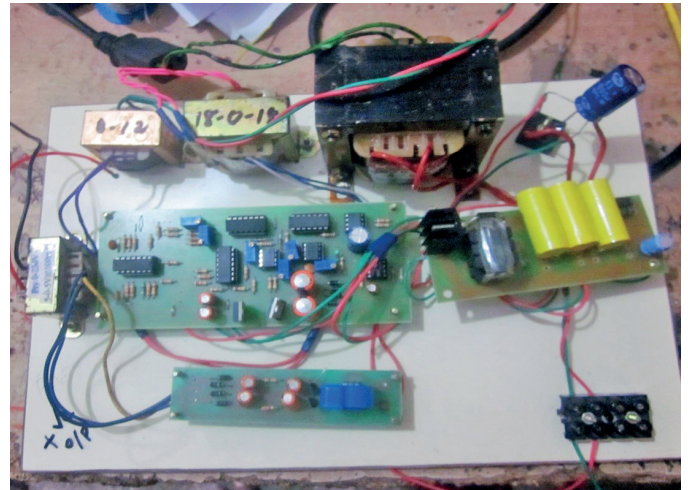


Fig. 25. Developed POELC

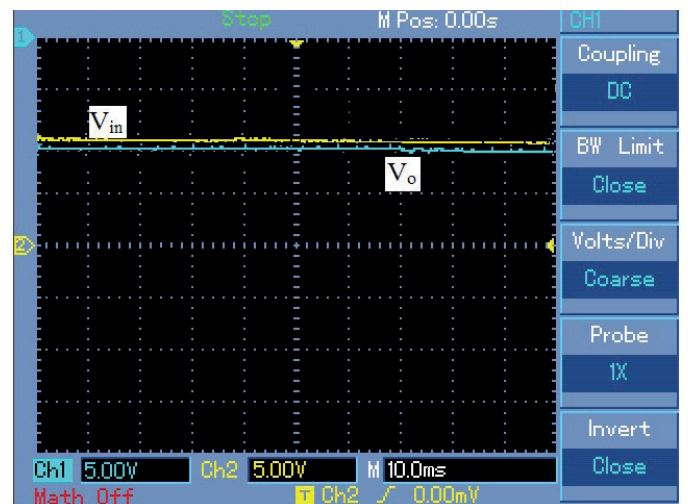


Fig. 26. Representative input and output voltages

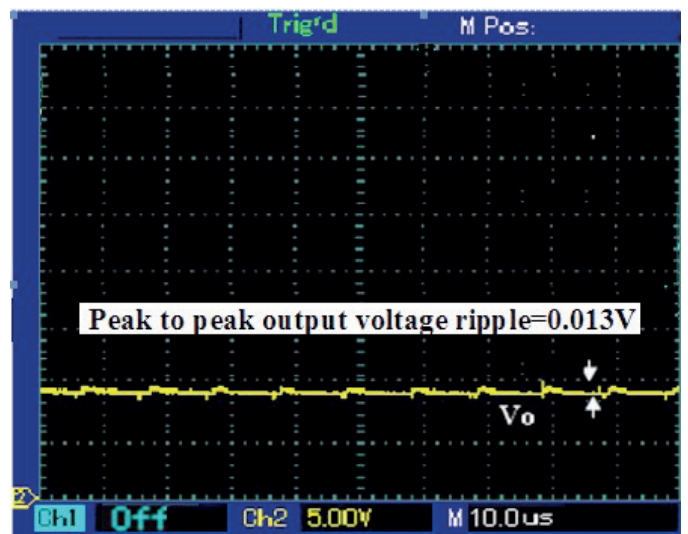


Fig. 27. Ripple study on output voltage

6. Conclusion

The systematic description of basic POELC and variable frequency ZVS-POELC has been presented in this paper firstly. The issues with the hard-switched POELC and the variable frequency ZVS-POELC have been addressed. A modified circuit topology to accommodate fixed frequency/ZVS-PWM operation in POELC has been insinuated. The inclusion of an auxiliary switch across the resonant inductor to create a free-wheeling stage within the quasi-resonant operation, enabled the converter to operate with a constant frequency and a much-reduced circulating energy.

REFERENCES

- [1] A. Kawa and R. Stala, "The flying-capacitor SEPIC converter with the balancing circuit", *Archives of Electrical Engineering* 65 (3), 411–424 (2016).
- [2] F.L. Luo and H. Ye, *Essential DC/DC Converters*, CRC Press, New York, 2006.
- [3] F.L. Luo and H. Ye, *Advanced DC/DC Converters*, CRC Press, New York, 2004.
- [4] F.L. Luo, "Positive output Luo converters: Voltage lift technique", *Proceedings of the IEE Electric Power Applications* 146 (4), 415–432 (1999).
- [5] J. Bojarski, R. Smolenski, P. Lezynski, and Z. Sadowski, "Diofantine equation based model of data transmission errors caused by interference generated by DC-DC converters with deterministic modulation", *Bull. Pol. Ac.: Tech* 64 (3), 575–580 (2016).
- [6] E. Jayashree and G. Uma, "Design and implementation of zero-voltage switching quasi-resonant positive output Luo converter using analog resonant controller UC3861", *IET Power Electronics* 4 (1), 81–88 (2011).
- [7] E. Jayashree and G. Uma, "Analysis, design and control of zero-voltage switching quasi-resonant positive output super lift Luo converter", *IET Power Electronics* 4 (1), 21–28 (2011).
- [8] E. Jayashree and G. Uma, "Soft-switched-controlled ultra-lift Luo converter", *IET Power Electronics* 4 (1), 151–158 (2011).
- [9] G. Hua, *Soft-Switching Techniques for Pulse-Width Modulated Converters*, Ph.D dissertation, Virginia Polytechnic Institute and State University, Virginia, 1994.
- [10] T. Meenakshi and N.S. Vanitha, "Modeling and simulation of novel stepped DC coupled quasi z-multilevel inverter for single-phase systems", *Archives of Electrical Engineering* 65 (3), 437–448 (2016).
- [11] K.H. Liu, R. Oruganti, and F.C.Y. Lee, "Quasi-resonant converters topologies and characteristics", *IEEE Transactions on Power Electronics* 2 (1), 62–71 (1987).
- [12] N. Mohan, T.M. Undeland, and W.P. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley and Sons, 2006.
- [13] M.K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, John Wiley and Sons, 2011.
- [14] M.K. Kazimierczuk, *Pulse-Width Modulated DC/DC Power Converters*, John Wiley and Sons, 2008.
- [15] S. Arulselvi, T. Archana, and G. Uma, "Design implementation of CF-ZVS-QRC using analog resonant controller UC3861 for aerospace applications", *International Conference on Power System Technology POWERCON'04*, Singapore, 1270–1275 (2004).
- [16] G. Uma, M. Shanthi, and C. Chellamuthu, "Design and implementation of constant frequency soft-switched regulated power supply for aerospace applications", *Proceedings of the IEEE International Symposium on Industrial Electronics ISIE'00* 1, Cholula, Mexico, 107–111 (2000).
- [17] S. Arulselvi, A.F. Biju, and G. Uma, "Design and simulation of fuzzy logic controller for a constant frequency quasi-resonant DC-DC converter", *ICISIP'04*, 472–476 (2004).
- [18] F.L. Luo and H. Ye, "Small signal analysis of energy factor and mathematical modeling for power DC-DC converters", *IEEE Transactions on Power Electronics* 22 (1), 69–79 (2007).
- [19] K.R. Kumar and S. Jeevananthan, "PI control for positive output elementary super lift Luo converter", *International Journal of Electrical Power and Energy Systems Engineering WASET'10* 3 (3), 130–135 (2010).
- [20] H. Anand and S. Jeevananthan, "Comparative study on hard- and soft-switched POESLL converters with design procedure", *Proceedings of the IEEE-Sponsored Third International Conference on Computation of Power, Energy, Information, and Communication ICCPEIC'14*, India, (2014).
- [21] M. Baszyński, "Low cost, high accuracy real-time simulation used for rapid prototyping and testing control algorithms on example of BLDC motor", *Archives of Electrical Engineering* 65 (3), 463–479 (2016).