

DOPANT-BASED CHARGE SENSING UTILIZING P-I-N NANOJUNCTION**Roland Nowak, Ryszard Jabłoński**

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Abstract

We studied lateral silicon p-i-n junctions, doped with phosphorus and boron, regarding charge sensing feasibility. In order to examine the detection capabilities and underlying mechanism, we used in a complementary way two measurement techniques. First, we employed a semiconductor parameter analyzer to measure I-V characteristics at a low temperature, for reverse and forward bias conditions. In both regimes, we systematically detected Random Telegraph Signal. Secondly, using a Low Temperature Kelvin Probe Force Microscope, we measured surface electronic potentials. Both p-i-n junction interfaces, p-i and i-n, were observed as regions of a dynamic behaviour, with characteristic time-dependent electronic potential fluctuations. Those fluctuations are due to single charge capture/emission events. We found analytically that the obtained data could be explained by a model of two-dimensional p-n junction and phosphorus-boron interaction at the edge of depletion region. The results of complementary measurements and analysis presented in this research, supported also by the previous reports, provide fundamental insight into the charge sensing mechanism utilizing emergence of individual dopants.

Keywords: nanosensor, silicon, p-i-n junction, dopant, Kelvin probe force microscope.

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1. Introduction

Rapid development of nanotechnology in the past 20 years also inevitably influences the field of metrology. The conventional sensors are not suitable anymore to be used in nano-sized objects, due to their extremely small size and appearance of non-classical (*i.e.*, quantum) effects. This is the main force driving the development of a new class of sensors – nanosensors. Shortly, such sensors are able to detect and transduce information about objects (*e.g.* DNA molecules, nanoparticles, elementary charges) or phenomena (*e.g.* emission of photon, tunneling) in nanoscale. Nanosensors are constantly finding new potential applications in medicine [1], biology, chemistry or physics [2]. Such sensors not only exhibit unique measuring capabilities, but are also expected to satisfy ever-growing demands regarding cost effectiveness and considerably reduced power consumption.

One of the main fields of interest is detection of single electrons or holes, mainly in nanoelectronics or nanophotonics. Such sensors play an important role in nano-circuits, where detection of changes of charge states is a critical and challenging task. Charge sensors are often constructed from various novel materials, including *carbon nanotubes* (CNTs) [3], graphene [4] or *molybdenum disulphide* (MoS₂) [5]. Such materials exhibit extraordinary properties, but fabrication processes are still challenging and the yield of successfully working devices remains relatively low.

In this work, we demonstrate a concept of charge (hole) [6] detection using a doped ultrathin silicon-on-insulator p-i-n junction. The p-i-n junctions, so far, are most commonly used in applications involving light (photons) – photodiodes [7] or solar cells [8]. The study presented here attempts to elucidate also the possibility of charge detection.

The devices were fabricated in a clean room environment, by means of standard, widely-used CMOS-compatible processes. Current-voltage (I-V) measurements, combined with the results of surface electronic potential maps measured by a *Low Temperature Kelvin Probe Force Microscope* (LT-KFM), reveal importance of individual dopants in nanostructured silicon. In particular, mutual interaction between *phosphorus* (P) and *boron* (B) turns out to be critical, thus classifying our device as a dopant-based sensor. As shown, such a P-B complex, when located at the boundary of depletion region, may determine operation of the entire device. In addition, it is evidenced that, in fact, our devices are two-dimensional. Finally, we shortly address future steps concerning structure basic simulation and outline how to significantly raise a level of fabrication controllability.

The paper is organized in the following way: the device fabrication is described in Section 2, in Section 3 we present and explain the results of I-V curves' and surface electronic potential measurements, providing a detection mechanism concept based on P-B mutual interaction; Section 4 shortly addresses future works towards first-principle simulations and well-controlled fabrication processes. Finally, Section 5 concludes the paper.

2. Device fabrication process

The fabrication process of prototype devices is shown schematically in Fig. 1. In the first step, an original *silicon-on-insulator* (SOI) wafer was cut into $1 \times 1 \text{ cm}^2$ squares (Fig. 1a). After that, the wafer squares were cleaned by means of ultrapure water, piranha solution ($\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$, ratio 3:1) and with a help of an ultrasonic generator. Next, the top silicon layer was thinned—the wafers were subjected to wet (with water vapor, 1000°C , $60 \text{ min} \times 2$) and dry (900°C , 22 min) thermal oxidation and subsequent etching by a hydrofluoric (HF) acid. As a result, the top silicon layer was around 20 nm thick, as confirmed by ellipsometer measurements (Fig. 1b). In the next step, we proceeded with *Electron Beam* (EB) Lithography patterning, in order to create the desired shape of devices. Silicon etching was done by dry *Reactive Ion Etching* (RIE). The anisotropic Si etching can use chemically reactive plasma (SF_6 24 SCCM, O_2 6 SCCM, RF Power 30 W, 15 s).

As shown in Fig. 1c, our devices consist of two relatively large SOI pads, connected by a constriction (channel). This specific shape arises from two reasons. First, our intention was to limit a parasitic capacitance that might affect LT-KFM measurements [9]. Such a capacitance occurs between the cantilever pad and the underlying silicon layer. In our case, this silicon layer does not exist and the cantilever pad moves mainly over the SiO_2 layer (buried oxide, BOX). Secondly, as we attempted to examine the effects caused by discrete dopant atoms (donors or acceptors), it was convenient to have a limited number of them (in a statistical sense).

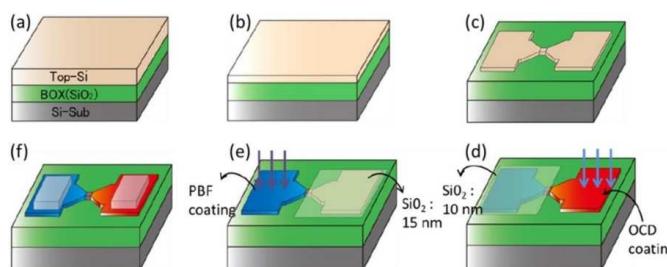


Fig. 1. $1 \times 1 \text{ cm}^2$ SOI wafers after cutting (a); the top silicon layer with a thickness of $\sim 20 \text{ nm}$ (b); the top silicon layer with an EB-patterned structure of p-i-n junction (c); phosphorus doping (d); boron doping (e); deposition of aluminum electrodes (f).

After having formed the shape of our devices, we doped donors and acceptors, in both cases by a standard thermal diffusion. First, we introduced *phosphorus* (P) donors into the n-type pad from spin-coated *silica glass* (OCD). During that, the p-type pad was covered by a thermally grown SiO_2 10-nm-thick mask (Fig. 1d). Such a thickness assured that no donors diffused through. Next, in a similar way, *boron* (B) acceptors were doped – Fig. 1e. This time, a *poly boron film* (PBF) was used as the boron source and the SiO_2 mask became 15 nm thick. Our design assumed that the p- and n-type pads were separated by a nominally 250-nm-wide i-type region. However, it must be mentioned that in reality, based on our experience, the alignment of masks during doping may be about 100 nm different than expected. Nevertheless, no overlap of doping masks occurred. P (donors) and B (acceptors) concentrations are: $N_D \approx 1 \times 10^{18} \text{ cm}^{-3}$ and $N_A \approx 1.5 \times 10^{18} \text{ cm}^{-3}$, respectively, as estimated from *secondary ion mass spectrometry* (SIMS). The i-region (nominally undoped) is not purely intrinsic – SOI wafers have a native low doping with B ($N_A \approx 1 \times 10^{15} \text{ cm}^{-3}$). However, since the estimated number of B atoms in the i-region is less than one per 10 nm³, it is reasonable to assume this region as intrinsic. Based on numerical simulations [31], it is expected that the lateral diffusion should not exceed several tens of nanometres. Finally, in order to passivate the surface and protect it from contamination, a thin layer (2 nm) of SiO_2 was grown on top (dry oxidation, 900°C, 15 s). We know from our previous experience that it does not influence KFM measurements in a noticeable way [10].

In the last step the aluminum electrodes were created, Fig. 1f, by means of conventional Physical Vapor Deposition (660°C, 6×10^{-4} Pa). The aluminum pads, shown in Fig. 1f, have a size of $600 \times 600 \mu\text{m}^2$ and are 150 nm thick. Depending on the type of measurement (e.g. floating or biased), we were able to apply a voltage.

The fabrication process was described in detail elsewhere [32].

3. Results and discussion

3.1. I-V characteristics in forward and reverse bias at low temperature

Figure 2a schematically shows the final device structure (the top Si thickness below 10 nm) together with the measurement setup for I-V characteristics (a semiconductor parameter analyzer, Agilent 4156C). The sample was inserted into a cryogenic high-vacuum (10^{-7} Torr) probe station (Lakeshore CPX-V). During measurements, the backgate was kept at $V_{BG} = 0$ V and, when needed, the voltage V_{SD} was altered. Fig. 2b demonstrates typical I-V curves taken at a room temperature. As it can be seen, the devices exhibit a typical diode behaviour for forward and reverse biases.

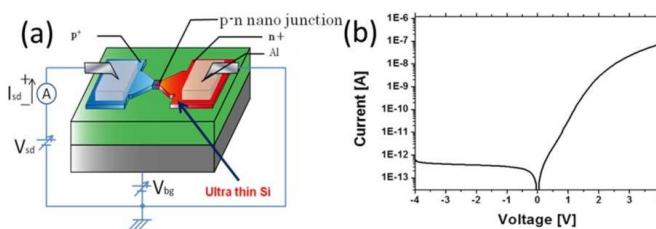


Fig. 2. The measurement setup used for I-V curves' measurements (a); a general I-V characteristic for forward and reverse biases (b).

The appearance of effects caused by individual dopant atoms is expected mainly at low temperatures, below 50 K. Fig. 3a and Fig. 3b show I-V curves taken again for forward and

reverse bias conditions. As demonstrated, the nanoscale p-i-n junction also exhibits a typical diode behaviour. However, the effect of parasitic resistance appeared and was reflected in the separation in the voltage domain – the threshold voltage of forward current shifted towards the positive direction (Fig. 3a), whereas the breakdown voltage shifted towards the negative direction (Fig. 3b). This is caused by the insulating behaviour of silicon and dopant freeze-out effect [6, 23], both due to a low temperature. In order to overcome such a voltage drop in the leads and to reach the junction area, a larger voltage must be applied.

The dashed ovals in Fig. 3a and Fig. 3b indicate current fluctuations, which are not observed at a room temperature. This current instability was confirmed by tracing the current as a function of time. As a result, we detected step-like features, resembling current switching known as *Random Telegraph Signal* (RTS) [11]. In Fig. 3a, repeatability of RTS onset was estimated to be at 9%, whereas in Fig. 3b – at 12%. RTS is well-known in submicron silicon MOSFETs [12, 13] and also other similar devices. In those structures, however, RTS is primarily caused by deep-level traps located near an Si/SiO₂ interface. This effect is not considered in our study, as it will be explained in Section 3.2.

Since the effects caused by individual dopants are more likely to emerge in smaller structures, we also measured a narrower device, with its nominal constriction width $W_C = 300$ nm. As seen in Fig. 3c, the current measured for several values of V_{SD} fluctuates mainly between two levels. Next, the raw RTS from Fig. 3c was digitized [14] and average time intervals were plotted as a histogram – Fig. 3d. There are two prominent durations of time intervals. These time intervals correspond to a dopant charge state (ionized or neutral), as will be described in Section 3.3.

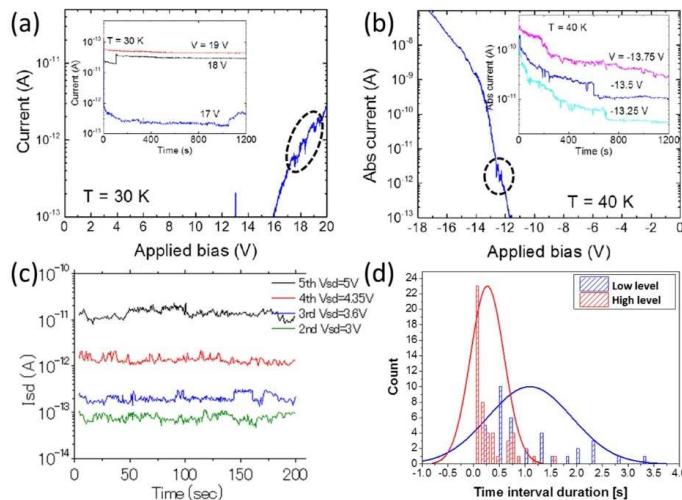


Fig. 3. I-V characteristics taken for the forward (a) and the reverse bias (b); the insets show RTS signals, mainly with two levels; (c) two-level RTS vs. time measured for different V_{SD} values; (d) a histogram of low and high current levels.

3.2. Observation of surface electronic potential by Kelvin probe force microscope

In order to further study the observed RTS, we carried out surface electronic potential measurements by a Kelvin probe force microscope [15] (Unisoku Co., Ltd.). It proved to be a powerful tool for characterization of nanodevices, able to achieve even atomic resolution [16]. We used gold-coated silicon cantilevers (Seiko Instruments Inc.), which were scanning ~10 nm over the device surface (the constant height mode). The p-i-n nanojunction was measured

in ultra-high vacuum (UHV, 10^{-9} Torr). Since our read-out setup is based on piezoelectric crystals, the common problems with light-induced effects [17] do not appear here. The backgate voltage was set to $V_{BG} = 0$ V and no bias was applied to the n- or p-type pads, as shown in Fig. 4a ($V_{REV} = 0$ V). The third voltage source, V_{KFM} , is a part of KFM circuit. It is used to nullify the electrostatic force, which builds up between the point charge (*e.g.* an ionized dopant) and the cantilever apex. The AFM image with a scan area for KFM mapping, marked by a dashed rectangle, is presented in Fig. 4b. Location of i-region (intrinsic) was estimated based on the topography profile and marked by orange dashed lines. It is important to mention here that, due to the measurement conditions, the device was mounted upside-down, so in fact electronic potential mapping was done from the n- towards the p-type pad.

First, we measured the p-i-n junction at a low temperature $T = 15$ K. The result is presented in Fig. 4c. As we anticipated, based on the device structure, we observed 3 major flat electronic potential sections, *i.e.* n-, i- and p-type regions. These regions are separated by localized-noise areas, which are marked in Fig. 4c by blue dashed ovals.

Based on the CMOS-compatible device fabrication process performed in a clean-room environment, a density of interface states is expected to be in the order of 10^{10} – 10^{11} cm $^{-2}$ eV $^{-1}$ or smaller [18, 19]. Thus, it can be estimated that in a 100×100 nm 2 area around a given interface (n-i or p-i), the number of interface traps (1–10) is negligible compared with the number of dopants (more than 200 dopants, P donors, and B acceptors). Based on that, dopant atoms (rather than interface states) are expected to give rise to any charging-related phenomena. Hence, in analogy to the RTS described in the previous section, these temporal electronic potential fluctuations are also caused by the dynamic charging/discharging of dopant atoms that are located within the n-i (and also i-p) interface.

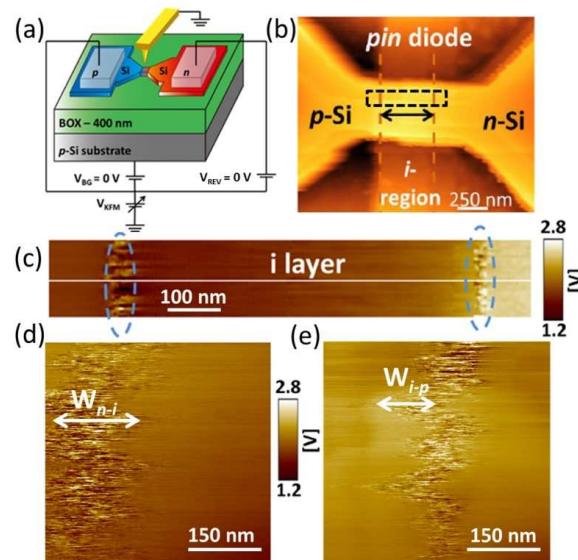


Fig. 4. The KFM measurement setup (a); an AFM picture of the measured device with a scan area for KFM measurements marked by a black rectangle (b); the surface electronic potential map with n-i and i-p interfaces marked by blue dashed ovals (c); the n-i (d) and i-p depletion regions (e).

In the next step, we performed electronic potential mapping around depletion regions (n-i or p-i interfaces) marked in Fig. 4c. The results for n-i and i-p junctions are presented in Figs. 4d and 4e, respectively. As it can be clearly seen, time-dependent electronic potential fluctuations

are again present. The next noticeable feature is that both interfaces have undulated shapes. Those wavy edges could be ascribed to the local arrangement of dopants within a given interface [20]. Finally, if we compare widths of both interfaces (marked in Figs. 4a and 4b), we observe that $W_{n-i} \approx 150$ nm, whereas $W_{i-p} \approx 100$ nm. The ratio of W_{n-i}/W_{i-p} corresponds to the ratio N_D/N_A (doping concentrations) and can only be observed in two-dimensional p-n (p-i-n) junctions [21].

3.3. Sensing mechanism based on dopant atoms at depletion region boundary of 2D p-n junction

As evidenced by the I-V curves (RTS) and KFM surface electronic potential maps (time-dependent fluctuations), p-i-n junctions exhibit dynamic behaviour. To clarify the underlying mechanism, a concept of active role of dopant atoms is introduced.

For simplicity we consider an n-i interface (shown in Fig. 4d), where phosphorus donors are interacting with boron acceptors. Taking into account the doping concentration (*i.e.* a higher concentration of phosphorus), it is likely that within the n-i interface region one boron acceptor is surrounded by many phosphorus donors, as it is schematically shown in Fig. 5a. In fact, these donors, due to the superposition of electronic potentials, create a cluster [22]. In such a cluster, an ionized boron (B^- state) acceptor raises a local electronic potential, limiting the flowing current. This situation corresponds to the ionized state, defined in the left part of Fig. 5c as a lower current level in RTS. On the other hand, when a hole is captured by a boron, its state is changed to the neutral (B^0 state). Consequently, the electronic potential within a cluster is lowered and a larger current may flow – Fig. 5b. This case reflects a neutralized state, *i.e.* a higher current level in RTS, as depicted in the right part of Fig. 5c.

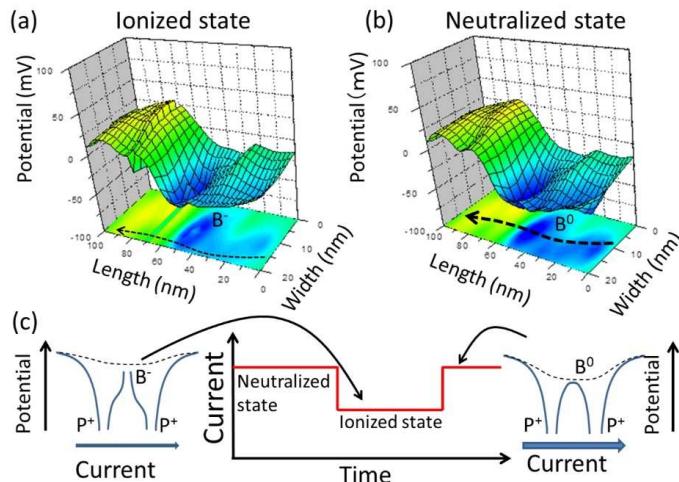


Fig. 5. A B acceptor in the ionized state (a); A B acceptor in the neutral state (b); A schematic of RTS with assigned the abovementioned states (c).

Detection of time-dependent noise, either RTS in I-V curves or electronic potential fluctuations in KFM images, would not be possible without the presence of deep-energy level dopants (primarily boron in this case). This is due to charge capture/emission time constants. For conventional dopants, these times are far beyond the detection limits [23]. Existence of such deep-energy level dopants is expected in ultra-small structures, ideally – in structures with reduced dimensionality [24, 25]. Considering this, together with a thickness of top-Si, we

concluded that the measured devices are truly two dimensional (2D). Another supporting fact comes directly from the KFM images and is related to the width of depletion regions, as discussed in Section 3.2.

The two-dimensional character of our device brings further consequences regarding its basic properties. It was theoretically predicted that the electric field within a depletion region, due to limited screening of host silicon, is very high [21] and penetrates outwards (confirmed experimentally [18, 28]), which may increase efficiency of electron-hole separation and, thus, increase sensitivity. Next, the electric field is also almost independent of the applied bias; therefore the breakdown voltage is considerably higher than in conventional p-n junctions. Moreover, the junction capacitance is very small, thus enabling to apply the device as a high-frequency diode, *e.g.* a photodetector. Finally, the width of depletion region is a linear function of applied voltage, which makes the adjustment also linear [21].

It is important to mention that the proposed model is valid for a cluster located favorably close to the edge of depletion region. Otherwise, charging/discharging boron atoms does not alter the local electronic potential sufficiently and RTS becomes unobservable. In other studies, for the purpose of RTS characterization, a concept of “sensitive region” was introduced [26, 27]. Such a region starts at the edge of depletion region (interface) and extends up to some length, usually several nanometres, towards the junction. Finally, the described model of sensing mechanism can also be adapted to the opposite case – when a phosphorus atom is embedded in a cluster of boron atoms.

4. Future steps

At a current level, location of dopants within a silicon lattice is random by nature and cannot be controlled. This is due to the fabrication processes, mainly the thermal diffusion used for introduction of dopant atoms into the host silicon. Therefore, as the next step of research, it is desired to produce such devices with a highest possible accuracy regarding a precise location of dopant atoms. In other words – by means of deterministic doping, *e.g.* using either ion implantation (SII) [29] or so called STM-Lithography [30].

Together with the experimental approach, theoretical studies are strongly desired. In particular, the basic electrical properties should be simulated. In fact, we performed first steps in this direction. We obtained first results performing ab initio calculations (Atomistix ToolKit) for a simple P-B-P complex inserted into a 2-nm-long Si nanowire (Fig. 6a) [31]. The results are presented in Fig. 6b. The *Density of States* (DOS) as a function of energy reveals that, despite a very short separation (0.5 nm), the ground states of P (a blue dashed line) and B (a red dashed line) atoms are preserved. It means that, even in such an extremely small structure, dopants can be ionized and work as charge traps. This finding further supports our model presented in the previous section. It is necessary, however, to carry out an ongoing study and simulation of larger structures with more dopants.

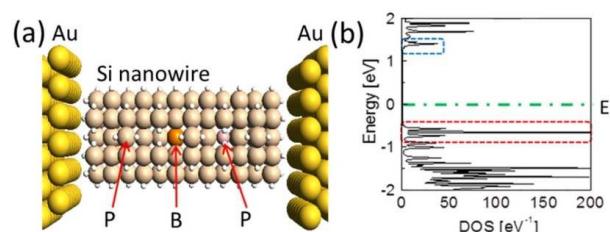


Fig. 6. The calculated structure containing a P atom surrounded by two B atoms (a); DOS with marked the ground states of donor and acceptor (b).

5. Conclusions

Summarizing, we have presented the results of basic studies devoted to modern p-i-n junctions. The examined devices, due to the used fabrication methods, offer a potentially high integration level for integrated circuits' applications.

The charge detection mechanism is ascribed to the charging/discharging of a deep-level boron atom. Such a charging/discharging phenomenon is manifested by current fluctuations (RTS) in the I-V characteristics and time-dependent electronic potential fluctuations in the KFM images. The mutual interaction between donors and acceptors has been proposed as a model of charge sensing mechanism.

Our devices combine unique properties due to reduced dimensionality and individuality of dopants, which exhibit deeper-energy levels. We believe that this work will contribute to a better understanding of new class of sensors – dopant-based nanosensors.

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