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On and Off Chip Capacitor Free, Fast Response, Low Drop-out Voltage Regulator

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***Abstract*—A low drop-out [LDO] voltage regulator with fast transient response which does not require a capacitor for proper operation is proposed in this paper. Recent cap-less LDOs do not use off chip capacitor but instead they use on chip capacitor which occupy a large area on the chip. In the proposed LDO, this on chip capacitor is also avoided. A novel secondary local feedback technique is introduced which helps to achieve a good transient response even in the absence of output capacitor. Further an error amplifier that does need compensation capacitor is selected to reduce the on chip area. Stability analysis shows that the proposed LDO is stable with a phase margin of 78°. The proposed LDO is laid out using Cadence Virtuoso in 180 nm standard CMOS technology. Post layout simulation is carried out and LDO gives $6mV/V$ and $360\mu V/mA$ line and load regulation respectively. An undershoot of $120\ mV$ is observed during the load transition from $0\ mA$ to $50\ mA$ in $1\ \mu s$ transition time, however LDO is able to recover within $1.4\ \mu s$. Since capacitor is not required in any part of design, it occupies only $0.010824\ mm^2$ area on the chip.**

***Keywords*—Voltage Regulator, Capacitor free LDO, Fast response, Area Efficient**

I. Introduction

THE longevity and performance of any electronic device highly depend on the quality of supply voltage. An ideal situation would be, a no change in the supply voltage level though there exist any fluctuations in power mains and load. However, in reality it is expected at least the static and dynamic variations in the supply voltage must be as minimum as possible. In this regard, LDO voltage regulators are gaining popularity. LDO is basically a linear voltage regulator with the minimum voltage drop between input and output terminals. A conventional LDO consists of an error amplifier, reference voltage, pass device, feedback network and output capacitor as shown in Fig. 1.

Linear Voltage Regulator is a negative feedback system where error amplifier continuously compares the feedback voltage with reference voltage and alters the conductance of pass device such that output voltage is maintained at the required level. The output capacitor acts like a charge storage and supplies the current when there is a sudden variation in the load current, so that error amplifier can take some time to respond. Hence larger the capacitance better the transient response. The quality of an LDO can be determined by the following aspects Area, Power efficiency, static parameters like line and load regulation, transient characteristics and noise immunity. However all parameters can not be improved together. There is always a trade-off among these parameters. For example, if quiescent current is reduced to improve the power efficiency, the transient response will be degraded. Hence depending on the applications, relevant parameters are targeted without causing much degradation on other parameters.

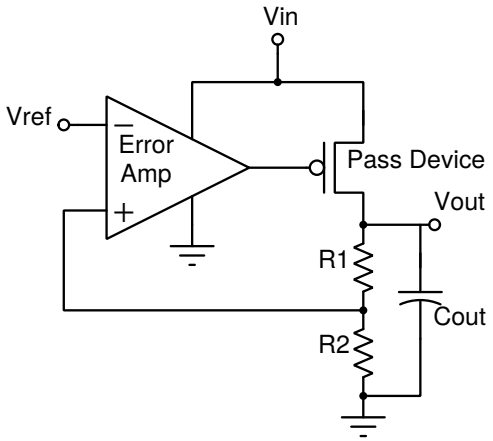

Fig. 1. Typical structure of a LDO

In any battery operated or portable devices, the area occupancy is a main design parameter. In conventional LDOs, an external large capacitor is used. This gives not only better transient response but also good stability. However such a large capacitor can not be integrated on the chip. Recent works [1]–[6] have proposed output capacitor-less LDOs where instead of using an external large capacitor, an internal on-chip capacitor is used. Though it avoids above mentioned drawbacks, it poses other challenges. The first one is on-chip capacitor occupies large area on chip and another is the degradation of transient response and stability. As previously mentioned, the large output capacitor constituted a dominant pole. Now since its removal, there is a need to create a dominant pole either at the output of error amplifier or at the final output. In LDO, the size of pass device is very large to accommodate low drop-out voltage and high load current. Hence the gate source parasitic capacitance of pass device is very large. During load transition, error amplifier has to charge this large capacitor. This effects the transient response of LDO. There have been many proposals to overcome this. In [7], [8] a Miller capacitor in series with a resistor is proposed. But it needs more space for the added passive elements. [9], [10] present an additional feedback loop consisting of a voltage spike detector and

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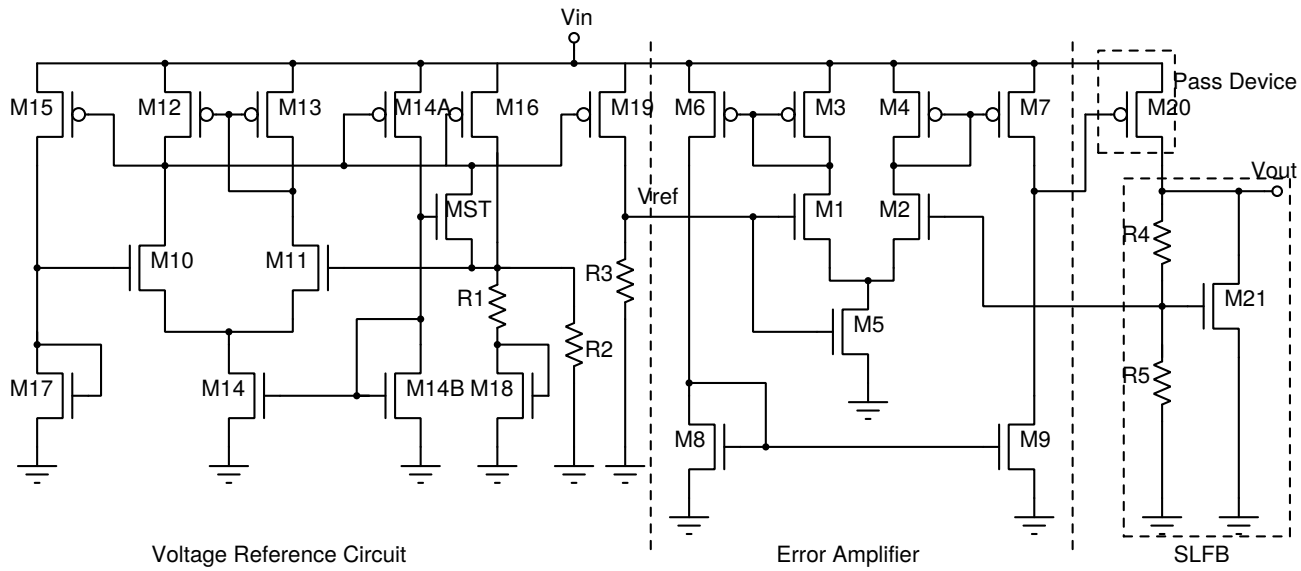

Fig. 2. Circuit diagram of proposed LDO

current amplifier which provides extra current to charge the parasitic capacitance of pass device. Though it improves the transient response and stability to some extend, it requires additional space, power and adds complexity. The authors of [11]–[13] suggest a flipped voltage follower in between error amplifier and pass device. Flipped voltage follower has better current sourcing capability but at the cost of higher quiescent current. Other proposed techniques mentioned in [14]–[16] are damping factor control frequency compensation (DFCFC), Q-reduction compensation and weighted current feedback (WCF). But DFCFC based LDO occupies a larger area and requires complex bias circuitry. The stability of the Q-reduction compensated LDO is poor when load is low. The loop gain of the LDO with WCF compensation is low hence the regulation performance is not satisfactory. To improve the power efficiency, author in [9] proposes a dynamic biasing technique where large biasing current is supplied only when there is any requirement. In all above works, a large on-chip capacitor has to be present for the proper operation of LDO which is a limiting factor in reducing the area occupancy on the chip. In the present work, a novel, area efficient LDO architecture is proposed, which is absolutely devoid of any capacitor.

Section 2 describes the construction and working principle of proposed LDO. The stability analysis of the LDO is elaborated in section 3. The result and discussion are given in section 4.

II. Design and Working Principle of Proposed LDO

Fig. 2 shows the complete circuit diagram of proposed LDO. Transistors from M_1 to M_9 form error amplifier, Transistors from M_{10} to M_{19} constitute voltage reference, M_{20} is the pass device and M_{21} with R_4, R_5 belong to Secondary Local Feedback [SLFB] block. Table I shows design parameter values.

A. Voltage Reference

A voltage reference provides a constant voltage irrespective of variations in temperature and supply voltage. A conventional band gap voltage [BGR] reference adds multiples of Proportional To Absolute Temperature [PTAT] and Complementary To Absolute Temperature [CTAT] voltages so that it exhibits zero temperature coefficient. However the demerit with the conventional BGR is it provides a voltage of nearly equal to 1.2V which is not suitable for modern CMOS technology regime. Another issue with the conventional BGR is it uses parasitic BJTs instead of using only MOSFETs. In [17] an alternate method is proposed in which CTAT and PTAT currents are added instead of voltages to produce a temperature independent current. Then it is passed through a resistor to obtain voltage. Though this method can produce a reference voltage less than 1V but it still uses parasitic BJTs to produce temperature independent voltage. In the proposed LDO, a MOSFET only topology is chosen for voltage reference circuit. MOSFET operation in sub-threshold region can be approximated to that of BJT. Hence diode connected MOSFET is used to produce PTAT and CTAT currents. MOSFET only voltage reference circuit [18], [19] is shown in Fig. 2.

MOSFET M_{17} and M_{18} are biased in sub-threshold region where drain current exhibits exponential exponential relationship with V_{GS}. The current through $R1$ is a PTAT current and current through $R2$ is a CTAT current. These currents are added to generate temperature independent current which flows through $R3$. The reference voltage produced by the reference circuit is given by

$$V_{ref} = [\frac{nkTln(m)}{qR_1} + \frac{V_A}{R_2}]R_3 \quad (1)$$

where n is slope factor, k is the Boltzmann's constant, q is the magnitude of electron charge, T is the temperature in Kelvin, m is the multiplication factor of M_{18} MOSFET and V_A is the voltage across $R2$. By selecting proper values of R_1,R_2 and R_3, V_{ref} can be set to required value. MOSFET MST is

added to avoid the reference circuit latching onto zero biasing current.

Fig. 3 shows the supply response of the reference circuit. The output voltage varies only $1\,mV$ for entire range of input voltage change. The temperature response is plotted in the Fig. 4. The output voltage variation was $14\,mV$ when temperature is swept from $0°$ to $100°$ C.

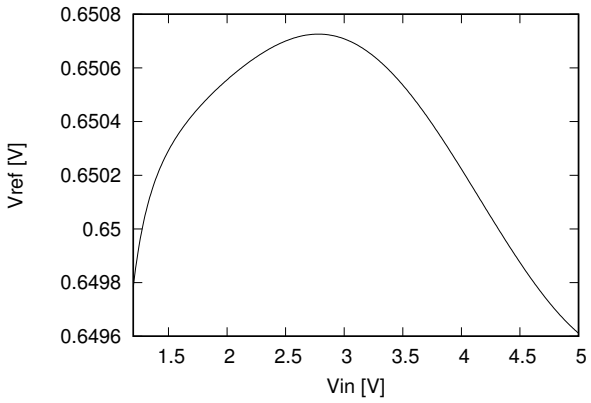

Fig. 3. Supply response of voltage reference

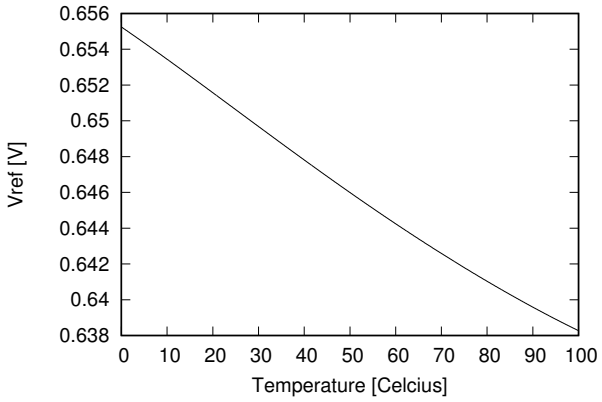

Fig. 4. Temperature response of voltage reference

B. Error Amplifier

Error amplifier decides many performance parameters of LDO. A two stage operational amplifier may do the job however it needs a compensation capacitor for stability. So an Operational Trans-conductance Amplifier [OTA] as shown in Fig. 2 is chosen which does not require compensating capacitor and also offers high open loop gain [20]. In the first stage, M_4 and M_3 are diode connected MOSFETs, hence dominant pole lies at the output node. In this way miller compensation capacitor is avoided.

C. LDO design

The challenging part in the design is to achieve stability and better transient response without using any on and off chip capacitor. To overcome this issue, a new method, secondary local feedback technique is used. Apart from main feedback, another feedback loop is introduced at the output terminal. The feedback consists of a NMOS transistor biased from resistor voltage divider network as shown in Fig. 2.

The worst condition occurs when load changes abruptly from minimum to maximum. At that time output voltage drops suddenly but if SLFB is used, whenever V_{out} falls, voltage at the gate of NMOS also falls. Since NMOS is in common source configuration, voltage at the drain (V_{out}) increases if voltage at the gate decreases. In this way the transient response of the LDO is improved which was earlier being done by an output capacitor.

TABLE I
DESIGN PARAMETER VALUES

Transistor	Aspect ratio
$M_1, M_2, M_6, M_7, M_8, M_9$	10
M_3, M_4, M_5	1
$M_{10} - M_{11}$	2
$M_{12}, M_{13}, M_{15}, M_{15}, M_{18}$	4
M_{14}	12
M_{17}	1
M_{19}	6
M_{20}	11111
M_{21}	20

III. Stability Analysis

The stability of the proposed LDO is investigated by determining the number of poles, zeros and their location on s-plane. Fig. 5 shows the small signal equivalent circuit of the LDO where loop is broken at the junction of $R4$ and $R5$. The following conventions are used in circuit analysis.
g_{mi} is the trans-conductance of i^{th} MOSFET.
r_{out} is output resistance at the output of OTA.
r_{21} is output resistance of M_{21}.
C_1,C_2 and C_3 are the parasitic capacitances of the first stage of OTA.
C_4 and C_5 are the parasitic capacitances of the output of OTA.
C_6 is the parasitic capacitance at the output of pass device.
C_7 is the parasitic capacitance of M_{21}.
$C_{2+3} = C_2 + C_3$, $C_{4+5} = C_4 + C_5$, $C_{6+7} = C_6 + C_7$.
The equivalent output resistance at the output of LDO is

$$R_o = r_{out}||r_n||R_l||(R_4 + R_5) \tag{2}$$

$$v_1 = -g_{m2}(X_{C2+3}||1/g_{m4}) = \frac{-g_{m2}v_p}{g_{m4} + sC_{2+3}} \tag{3}$$

$$v_2 = \frac{-g_{m7}v_1 r_{ota}}{1 + sC_{4+5}r_{ota}} = \frac{g_{m7}v_p g_{m2} r_{ota}}{(1 + sC_{4+5}r_{ota})(g_{m4} + sC_{2+3})} \tag{4}$$

$$v_{out} = -(g_{m20}v_2 + g_{m21}v_b)\frac{R_o}{1 + sC_{6+7}R_o}$$

$$= \frac{-R_o g_{m20} v_2}{1 + sC_{6+7}R_o} - \frac{R_o g_{m21} v_b}{1 + sC_{6+7}R_o} \tag{5}$$

$$v_b = \frac{v_{out}R_5}{R_4 + R_5} \tag{6}$$

$$= -\frac{R_o R_5 g_{m20} v_2}{[(1 + sC_{6+7}R_o)(R_4 + R_5) + R_o R_5 g_{m21}]}$$

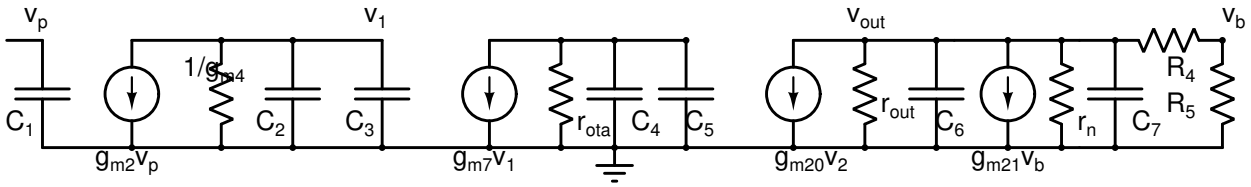

Fig. 5. Small signal equivalent circuit diagram of proposed LDO

$$\frac{v_b}{v_p} = -\frac{(r_{out}||r_n||R_l||(R_4+R_5))}{((1+sC_{6+7}(r_{out}||r_n||R_l||(R_4+R_5)))} X \frac{R_5 g_{mp} g_{m7} g_{m2} r_{ota}}{(R_4+R_5)+(r_{out}||r_n||R_l||(R_4+R_5))R_5 g_{mn})} X \frac{1}{(1+sC_{4+5}r_{ota})(g_{m4}+sC_{2+3})} \quad (7)$$

The system has three poles of concern. The parasitic capacitance, which is formed due to pass transistor is the largest among all the parasitic capacitances. The output impedance of LDO is dependent on the load but it has been ensured that always impedance seen at the output of error amplifier is much larger than the impedance seen at the regulator output [which is verified using simulation as explained in the next paragraph]. Hence the pole at error amplifier output is a dominant one. The expression for three poles are given below.

$$P_1 = \frac{1}{2\pi C_{4+5} r_{ota}} \quad (8)$$

$$P_2 = \frac{1}{2\pi C_{6+7} R_o} \quad (9)$$

$$P_3 = \frac{g_{m4}}{2\pi C_{2+3}} \quad (10)$$

Typically a regulator supplies voltage to a long on-chip network which introduces considerable load capacitance, which may vary from several $0\ pF$ to $50\ pF$. Therefore stable operation of the proposed regulator has been verified by simulating it for various load capacitances and loads. The loop gain and phase response of proposed LDO for an output capacitance of $0\ pF$ under the load of $10\ \mu A$, $25\ mA$ and $50\ mA$ are shown in Fig. 6[a] and Fig. 6[b]. Similarly, Fig. 6[c], Fig. 6[d] and Fig. 6[e], Fig. 6[f] show the loop gain and phase responses for the output capacitances of $25pF$ and $50pF$ respectively. It is evident from the plots that LDO is stable in all the cases. Pole zero analysis for the proposed LDO, for above mentioned values of output capacitors and loads has been carried out using Cadence simulation tool and all the poles and zeros of concern along with phase margin and unity gain bandwidth have been tabulated in Table II . It can be seen from the table that stability of LDO is not disturbed by the presence of output parasitic capacitance.

IV. Results and Discussion

The proposed LDO was laid out in 180 nm standard CMOS technology using Cadence Virtuoso tool. The post layout results are summarized in this section. Line regulation of LDO for different loads are shown in Fig. 7[a]. The average line regulation was found to be $6\,mV/V$. Fig. 7[b] shows the load regulation of proposed LDO. The change in output voltage was $360\ \mu V/mA$. To measure load transient response, LDO was subjected to load change from 0A to 50 mA with a transition time of $1\mu s$. The recorded under-shoot, over-shoot and average recovery time were respectively $130\,mV$, $120\,mV$ and $1.4\,\mu s$ as shown in Fig. 7[c]. This reduction in recovery time and magnitude of over and undershoot even in the absence of any on or off chip capacitor was due to the presence of SLFB. The secondary feedback loop is faster than the main feed back which helps in quick recovery of output voltage as well as prevents it from drooping heavily. To measure the line transient, a step signal of $0.2\ V$ with $1\ \mu A$ transition time was applied along with the input $1.3\,V$. The LDO exhibited a fluctuation of around $40\,mV$. The recovery time was found to be $1.5\,\mu s$. The line transient response is shown in Fig .7[d].

The robustness of the proposed LDO against Process variations and mismatch was tested using Monte-Carlo analysis. The line regulation of proposed LDO was measured under process variations and mismatch. The mean value of line regulation was $6.7\ mV/V$. Load regulation of the LDO was also verified using Monte-Carlo simulation. The mean value of load regulation was measured to be $106\,\mu V/mA$. Fig. 8[a] and Fig. 8[b] show Monte-Carlo histogram plot of line and load regulation variations for different samples respectively. The mean value of line and load regulation obtained from Monte-Carlo simulation were matching with the nominal values of the LDO. Finally one more set of Monte-Carlo simulation was carried out to investigate the effect of process variations and mismatch on load transient response. The magnitude of undershoot during load transition from $0\,A$ to $50\,mA$ was plotted for different samples as shown in Fig. 8[c]. The mean variation was found to be $120\ mV$. The above results prove that the proposed LDO is robust. The layout of proposed LDO with reference voltage is shown in Fig. 9 which occupies an area of $0.122\ mm\ X\ 0.120\ mm$. If reference voltage is omitted then LDO area becomes $0.132\,mm\,X\,0.082\,mm$. This drastic reduction in area is because of the absence of on chip capacitor in the design.

Table III shows the performance comparison of proposed LDO with the recent works. Dropout voltage depends on size of pass transistor and maximum driving current. In the proposed LDO, $300\,mV$ dropout voltage was chosen to reduce the area occupancy. The quiescent current is the sum of biasing current and current flowing through feedback resistors. The proposed LDO consumes $70\ \mu A$, out of which $58\ \mu A$ flows into feedback resistors. It can be reduced by increasing value of feedback resistors. However it not only needs more area on chip but also degrades the stability. The settling time of

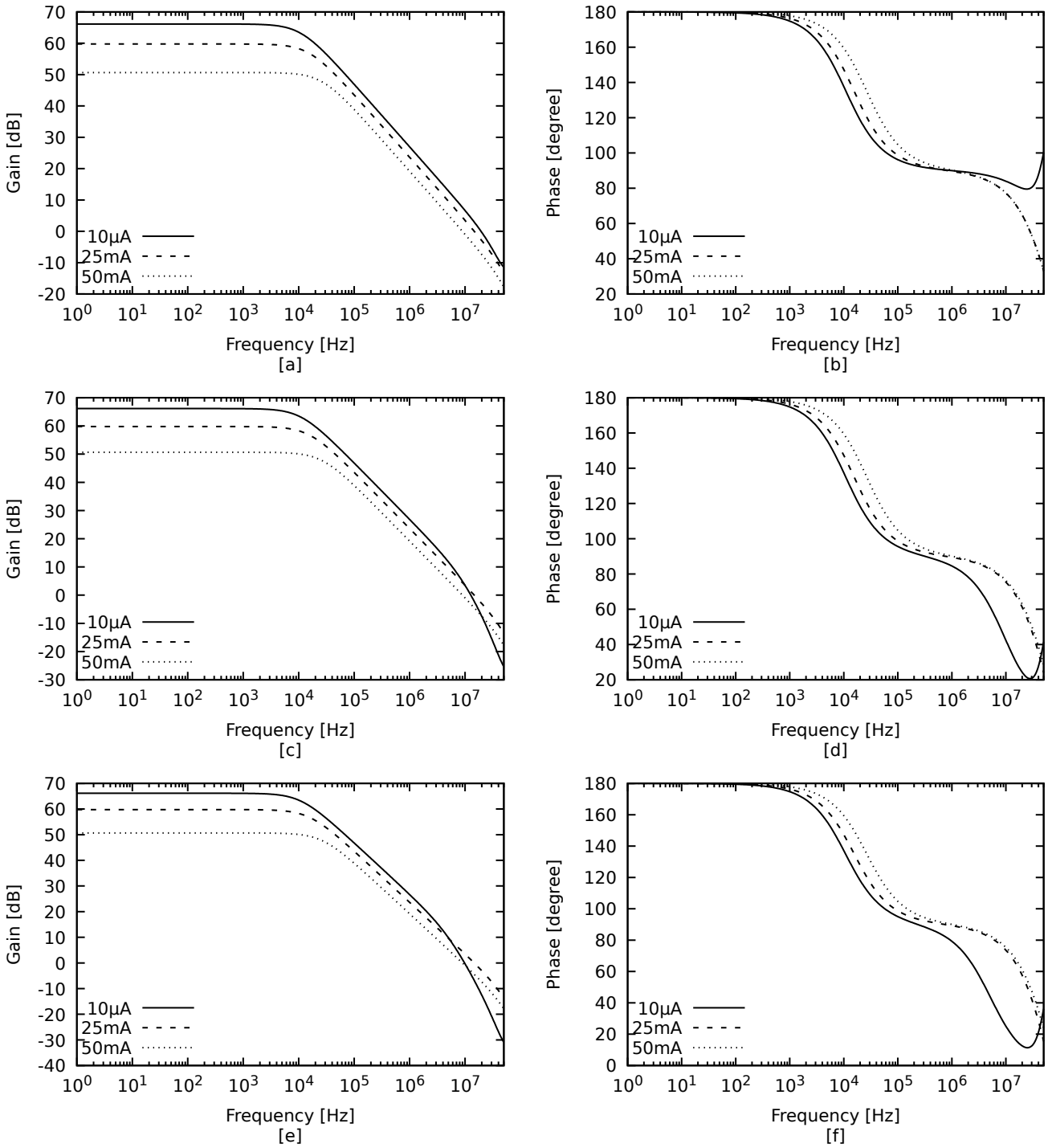

Fig. 6. [a] Loop gain response for $C_{out} = 0\,pF$ [b] Loop phase response for $C_{out} = 0\,pF$ [c] Loop gain response for $C_{out} = 25\,pF$ [d] Loop phase response for $C_{out} = 25\,pF$ [e] Loop gain response for $C_{out} = 50\,pF$ [f] Loop phase response for $C_{out} = 50\,pF$

the proposed LDO is very small when compared with other LDOs. Though the work proposed in [1], [6] and [7] have lesser settling time, either a large on-chip capacitor or high quiescent current is used. With respect to magnitude of undershoot voltage parameter, only the work in [1], [7] and [9] show better performance than the proposed LDO. However in [1], this improvement is due to the large on-chip capacitor and in [7] and [9] the maximum load is only $10\ mA$ and $0.5mA$ respectively. In the output capacitance parameter, the proposed LDO stands clearly distinguishable from other state of art LDOs.

TABLE II
STABILITY ANALYSIS

Capacitor	Load	Pole-1	Pole-2	Pole-3	Zero-1	Phase Margin	Bandwidth
0 pF	10 μA	-2.28E7+i1.79E7	-2.28E7-i1.79E7	-6.03E7	-6.06E7	80°	19.4 MHz
0 pF	25 mA	-2.6E7+i1.37E7	-2.6E7-i1.37E7	-6.03E7	-6.01E7	71°	14.63 MHz
0 pF	50 mA	-1.24E7	-4.29E7	-6.02E7	-5.99E7	78.6°	8.9 MHz
25 pF	10 μA	-4.24E6+i1.34E7	-4.24E6-i1.34E7	-6.03E7	-6.06E7	35°	12.7 MHz
25 pF	25 mA	-2.38E7+i1.6E7	-2.28E7-i1.6E7	-6.03E7	-6.01E7	68°	14.6 MHz
25 pF	50 mA	-1.28E7	-4.1E7	-6.02E7	-5.9E7	77°	8.9 MHz
50 pF	10 μA	-2.27E6+i1E7	-2.27E6-i1E7	-6.03E7	-6.01E7	25°	9.7 MHz
50 pF	25 mA	-2.13E7+i1.8E7	-2.13E7-i1.8E7	-6.03E7	-6.01E7	66°	14.5 MHz
50 pF	50 mA	-1.33E7	-3.9E7	-6.02E7	-5.99E7	77°	8.9 MHz

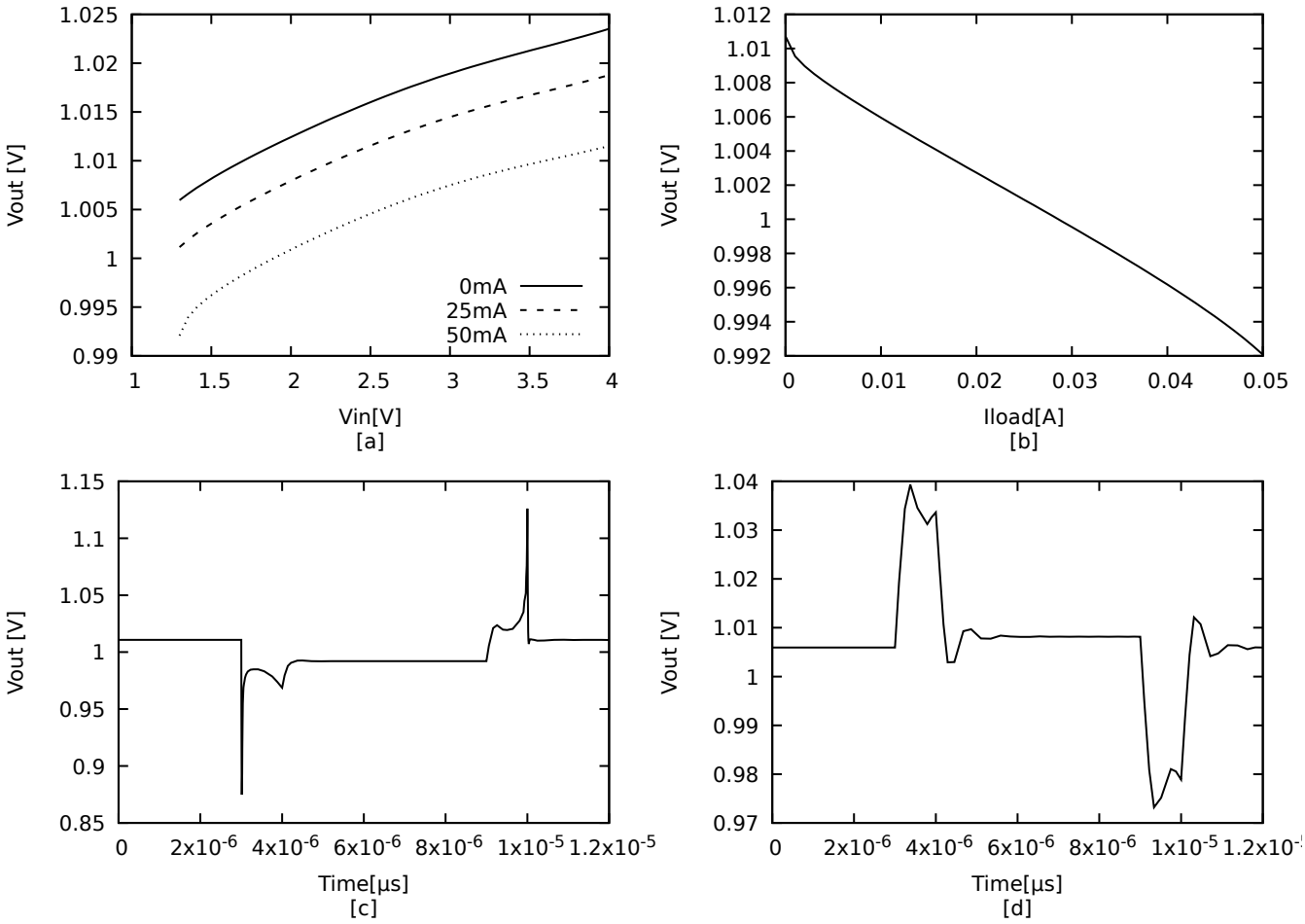

Fig. 7. [a] Line regulation of the LDO [b] Load regulation of the LDO [c] Load transient response of the LDO [d] Line transient response of the LDO

TABLE III
PERFORMANCE COMPARISON OF PROPOSED LDO WITH RECENT LDOS

Parameter	[1]	[3]	[4]	[5]	[6]	[7]	[9]	This work
Technology [μm]	0.18	0.5	0.35	0.35	0.11	0.065	0.18	**0.18**
Dropout Voltage[mV]	200	200	200	200	200	250	200	**300**
Max. load [mA]	100	100	100	100	200	10	0.5	**50**
Quiescent Current [μA]	31.6	78.21	15	15	4.5	346	10.5	**70**
Settling Time [μs]	1.3	2.5	2	–	0.8	0.4	3.5	**1.4**
Δ **Vout**[mV]	42	135	148	270	260	41.6	26	**130**
Cout [pF]	100	100	100	6.8	100	16+470	100	**0**
Area [mm^2]	–	0.7	0.043	0.047	0.09	–	0.012	**0.0108**

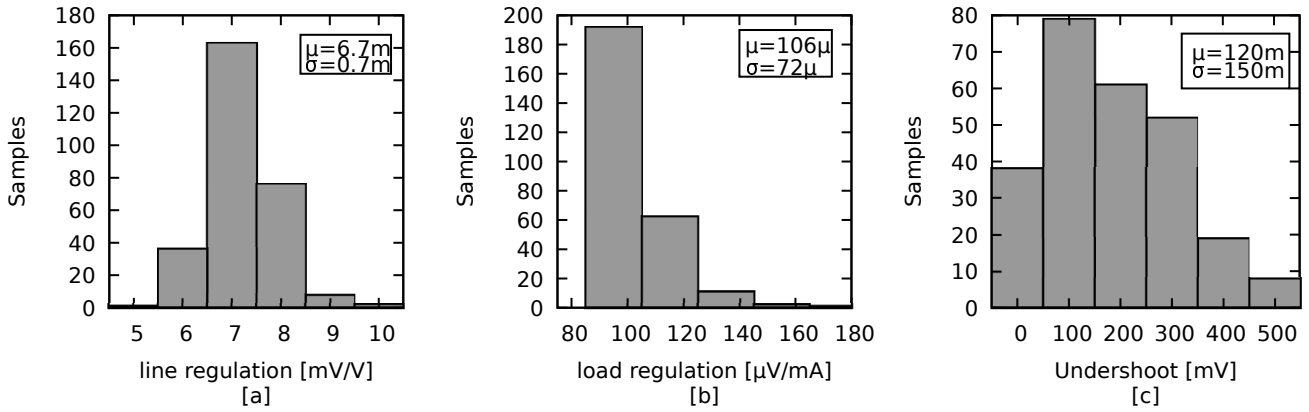

Fig. 8. [a] Histogram plot of the line regulation variation for different samples [b] Histogram plot of the load regulation variation for different samples [c] Histogram plot of the under-shoot voltage variation for different samples

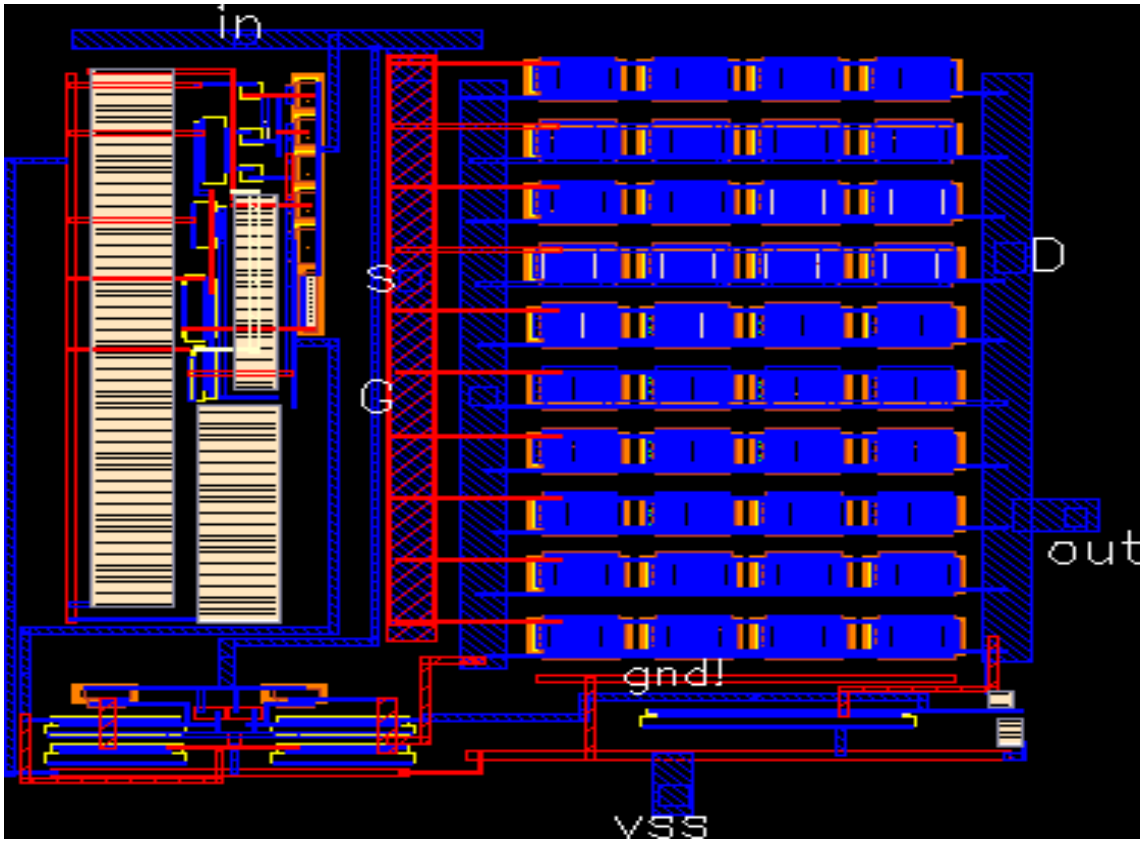

Fig. 9. Layout of the proposed LDO

V. Conclusion

In the proposed work, a novel LDO architecture is presented which does not require a capacitor to function properly. The introduced new technique, local secondary feedback ensures better transient response even though no capacitor is used. The circuit occupies a very small area on the chip and consumes a low quiescent current making suitable for low power and area constrained applications.

References

[1] Y. Zeng, Y. Li, X. Zhang, and H.-z. Tan, "A push-pulled fvf based output-capacitorless ldo with adaptive power transistors," *Microelectronics Journal*, vol. 64, pp. 69–77, 2017.

[2] A. Saberkari, E. Alarcón, and S. B. Shokouhi, "Fast transient current-steering cmos ldo regulator based on current feedback amplifier," *Integration, the VLSI Journal*, vol. 46, no. 2, pp. 165–171, 2013.

[3] J. Hinojo, C. Luján-Martínez, A. Torralba, and J. Ramírez-Angulo, "Internally compensated ldo regulator based on the cascoded fvf," *Microelectronics Journal*, vol. 45, no. 10, pp. 1268–1274, 2014.

[4] S.-K. Kao, Y.-Z. Lee, C.-Y. Ku, and H.-C. Cheng, "Output capacitor-free low-dropout regulator with fast transient response and ultra small compensation capacitor," *Microelectronics Journal*, vol. 56, pp. 134–141, 2016.

[5] X. Ming, N. Li, X.-m. Zhang, Y. Lu, Z.-k. Zhou, and Z. Wang, "A capacitor-less ldo regulator with dynamic transconductance enhancement technique," *Analog Integrated Circuits and Signal Processing*, vol. 84, no. 3, pp. 433–444, 2015.

[6] J. Yeo, K. Javed, J. Lee, J. Roh, and J.-D. Park, "A capacitorless low-dropout regulator with enhanced slew rate and 4.5ua quiescent current," *Analog Integrated Circuits and Signal Processing*, vol. 90, no. 1, pp. 227–235, 2017.

[7] Y. Yosef-Hay, D. Ø. Larsen, P. L. Muntal, and I. H. Jørgensen, "Fully integrated, low drop-out linear voltage regulator in 180 nm cmos," *Analog Integrated Circuits and Signal Processing*, pp. 1–10, 2017.

[8] C.-M. Chen, T.-W. Tsai, and C.-C. Hung, "Fast transient low-dropout voltage regulator with hybrid dynamic biasing technique for soc application," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 9, pp. 1742–1747, 2013.

[9] J. Esteves, J. Pereira, J. Paisana, and M. Santos, "Ultra low power capless ldo with dynamic biasing of derivative feedback," *Microelectronics Journal*, vol. 44, no. 2, pp. 94–102, 2013.

[10] Y.-i. Kim and S.-s. Lee, "A capacitorless ldo regulator with fast feedback technique and low-quiescent current error amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 6, pp. 326–330, 2013.

[11] C. Li and P. K. Chan, "Fvf ldo regulator with dual dynamic-load composite gain stage," *Analog Integrated Circuits and Signal Processing*, pp. 1–10, 2017.

[12] S. J. Yun, J. S. Kim, and Y. S. Kim, "Capless ldo regulator achieving-76 db psr and 96.3 fs fom," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2016.

[13] X. Han, T. Burger, and Q. Huang, "An output-capacitor-free adaptively biased ldo regulator with robust frequency compensation in 0.13 μm cmos for soc application," in *Circuits and Systems (ISCAS), 2016 IEEE International Symposium on*. IEEE, 2016, pp. 2699–2702.

[14] K. N. Leung and P. K. Mok, "A capacitor-free cmos low-dropout regulator with damping-factor-control frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, 2003.

[15] S. K. Lau, P. K. Mok, and K. N. Leung, "A low-dropout regulator for soc with q-reduction," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 658–664, 2007.

[16] X. L. Tan, S. S. Chong, P. K. Chan, and U. Dasgupta, "A ldo regulator with weighted current feedback technique for 0.47 nf–10 nf capacitive load," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2658–2672, 2014.

[17] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A cmos bandgap reference circuit with sub-1-v operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, 1999.

[18] S. Hongprasit, W. Sa-Ngiamvibool, and A. Aurasopon, "Design of bandgap core and startup circuits for all cmos bandgap voltage reference," *PRZEGLAD ELEKTROTECHNICZNY*, vol. 88, no. 4 A, pp. 277–280, 2012.

[19] C. J. B. Fayomi, G. I. Wirth, H. F. Achigui, and A. Matsuzawa, "Sub 1 v cmos bandgap reference design techniques: a survey," *Analog Integrated Circuits and Signal Processing*, vol. 62, no. 2, pp. 141–157, 2010.

[20] P. Pérez-Nicoli, F. Veirano, P. C. Lisboa, and F. Silveira, "Low-power operational transconductance amplifier with slew-rate enhancement based on non-linear current mirror," *Analog Integrated Circuits and Signal Processing*, vol. 89, no. 3, pp. 521–529, 2016.