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Phase compensation scheme for feedforward linearized CMOS operational transconductance amplifier

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Abstract. In the paper, a feedforward linearization method for differential-pair operational transconductance amplifier (OTA) is discussed. The proposed technique is developed using simple differential pair transconductors and linear reference resistor. The concept leads not only to very efficient linearization of a transfer characteristic of the OTA but also offers the possibility of effective phase compensation. Due to this, the circuit can be used in applications requiring precise phase response (e.g. filters). SPICE simulations show that for the circuit working with a ±1.25V power supply, total harmonic distortion (THD) at $0.8V_{pp}$ is less then 0.1% in comparison to 10.2% without linearization. Moreover, the input voltage range of linear operation is increased. Power consumption of the overall circuit is 0.94mW. The 3rd order elliptic filter example has been designed and simulated. It turns out that the proposed compensation scheme significantly improves the performance of the filter at higher frequencies.

Keywords: CMOS transconductor, phase compensation, active-error feedforward.

1. Introduction

CMOS transconductance elements are useful building blocks for the design of many analog and analog-digital signal processing systems. Such applications (e.g. active filters and tranconductance multipliers) usually require very linear voltage-to-current converters (transconductors) or operational transconductance amplifiers (OTAs) [1–4]. One of the simplest and most widely used transconductors is a source-coupled differential pair [4]. It is commonly known that an application of the feedforward technique enables to improve performance of many analog signal processing circuits. This technique is widely used to reduce nonlinear distortion in amplifiers [5–12]. Moreover, it is successfully employed to frequency compensation of operational amplifiers and OTAs [13–16]. Other phase compensation schemes for multistage amplifiers have also been reported in literature [17–19].

Several techniques for improving the linearity properties of CMOS transconductors of OTAs based on the source-coupled differential pairs (both symmetrical and unsymmetrical) have recently been proposed [20–34]. These techniques employ MOS transistors operating both in saturation and triode regions. Such linearization methods as adaptive biasing (e.g. [25]), source degeneration (e.g. [29]), and current differencing lead to effective linearization (e.g. [28]), current addition (e.g. [23]), however, at the expense of increased power consumption and, usually, reduced transconductance factor and power efficiency (defined as the maximum linear output current divided by the total bias current [4]).

In this work, a novel highly linear operational transconductance amplifier (OTA) is proposed. The circuit uses, as basic building blocks, simple differential pair transconductors. The linearization follows by employing an active-error feedforward scheme. The error signal is generated using an additional differential pair transconductor and a resistor which is assumed to be linear. This resistor can be an external one or it can be implemented as an monolitic element e.g. using a high resistive poly technology. Moreover, this resistor can be tuned digitally using an appropriate matrix of switches and reference resistors.

It follows that the linearization circuitry itself offers an interesting phase compensation scheme, which is different from the ones described in the literature so far [16,26,27]. Moreover, the linearized circuit topology ensures that no right-half plane (RHP) zeros are present. Obviously, some of the previously reported compensation schemes can be also applied to the proposed transconductor. In practice, the method [26] is preferred for its simplicity.

The proposed technique gives effective linearization and is free of drawbacks mentioned in the previous paragraph. In particular, it allows us to implement the OTA circuit which has extremely low power consumption, extended linear range of operation as well as good transconductance tuning capability. Moreover, the effective phase compensation can be easily applied, which makes the circuit suitable for high-frequency applications (e.g. filters).

The paper is organized as follows. In Section 2, a description of the proposed linearization method is presented. In Section 3, a frequency response of the linearized circuit is analysed in detail using the transconductor model that comprises parasitic capacitors and conductances. Section 4 presents the circuit realization of the linearized differential pair OTA. In Section 5, the SPICE simulation results of the OTA are discussed, including THD and Monte Carlo analysis. In Section 6, the example of 3rd order elliptic filter is design and simulated. Section 7 concludes the paper.

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2. Description of feedforward linearization method

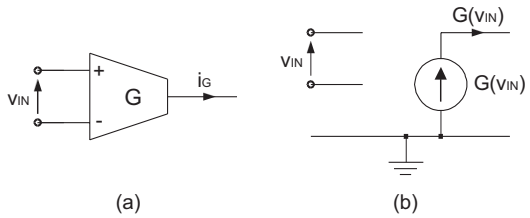

Fig. 1. Nonlinear model of transconductance element: (a) symbolicrepresentation, (b) AC-equivalent model

For the purpose of the subsequent analysis we will represent the nonlinear transfer characteristic of transconductor using power series expansion. Let i_G denotes the output current of the transconductor, while v_{IN} is the differential input voltage of the transconductor as shown in Fig. 1. Then we have

$$i_G(v_{IN}) = \sum_{n=1}^{\infty} g_n v_{IN}^n(t) = G(v_{IN}) \tag{1}$$

where coefficients g_n are defined as

$$g_n = \frac{1}{n!} \frac{d^n G(v_{IN})}{dv_{IN}^n}\bigg|_{v_{IN}=0}. \tag{2}$$

By definition, coefficient g_1 is the transconductance g_m of the amplifier.

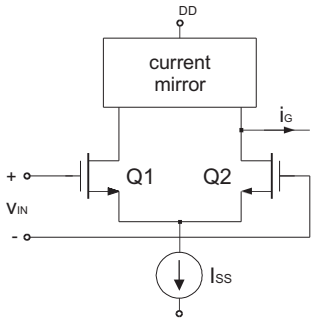

Fig. 2. Simple CMOS differential pair transconductor

Consider the simple CMOS differential pair transconductor shown in Fig. 2. It can be shown, using square-law MOS transistor modelling, (e.g. [35]) that its normalized transfer characteristic around zero is:

$$i_G(x) = 2I_{SS} x\sqrt{1-x^2} \tag{3}$$

where x is a normalized input voltage defined as $x = v_{IN}2(V_{GS} - V_T)$, with v_{IN} being a differential input voltage, V_{GS} and V_T — gate-source DC voltage and threshold voltage, respectively; I_{SS} is the biasing current of the differential pair. Actually, formula (3) is valid for $|x| \leqslant \sqrt{2}/2$. For larger x the transfer characteristic saturates. The corresponding power series expansion is of the form:

$$i_G(x) = 2I_{SS}\left(x - \frac{1}{2}x^3 - \frac{1}{8}x^5 - \frac{1}{16}x^7 - \frac{5}{128}x^9 \ldots\right). \tag{4}$$

Figure 3. shows the concept of transconductance amplifier linearization based on active-error feedforward method. All amplifiers $G^{\langle 1\rangle}$, $G^{\langle 2\rangle}$, $G^{\langle 3\rangle}$, modelled as in Fig. 1, are assumed to be identical. Their transfer characteristics are described by the power series expansion (1). Moreover, it is assumed that resistor R in Fig. 3 is linear and equal to $1/g_m$. In practice, e.g. in integrated circuit implementations some technologies offer high resistive poly which can be used to realize resistor R. Alternatively, such a resistor can be treated as an external (discrete) element.

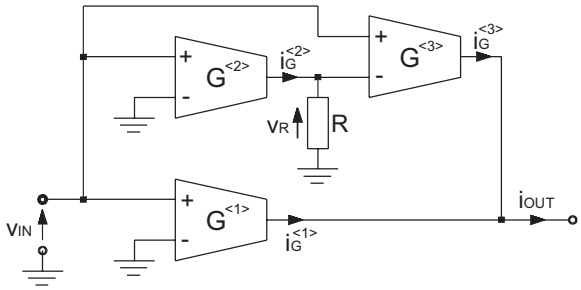

Fig. 3. Three-block feedforward transconductance amplifier

Using (1), the output current i_{OUT} of the overall circuit in Fig. 3. can be written as follows:

$$i_{OUT}(t) = \sum_{n=1}^{\infty} g_n[v_{IN}(t)]^n + \sum_{n=1}^{\infty} g_n[v_{IN}(t) - v_R(t)]^n \tag{5}$$

where

$$v_R(t) = g_1^{-1} \sum_{n=1}^{\infty} g_n[v_{IN}(t)]^n. \tag{6}$$

This means that the voltage at the input of the transconductor $G^{\langle 3\rangle}$ (working as an error amplifier) equals $v_{IN}(t) - v_R(t) = v_{IN}(t) - g_1^{-1}\sum_{n=1}^{\infty} g_n[v_{IN}(t)]^n = -g_1^{-1}\sum_{n=2}^{\infty} g_n[v_{IN}(t)]^n$. Hence, we obtain

$$i_{OUT}(t) = \sum_{n=1}^{\infty} g_n[v_{IN}(t)]^n + \sum_{n=1}^{\infty} g_n\left[-g_1^{-1}\sum_{k=2}^{\infty} g_k[v_{IN}(t)]^k\right]^n. \tag{7}$$

Normally, $v_{IN}(t) - v_R(t)$ is much smaller than the input voltage of transconductors $G^{\langle 1\rangle}$ and $G^{\langle 2\rangle}$, which allows us to neglect the higher order terms in the output current of $G^{\langle 3\rangle}$. This leads to the following approximation:

$$i_{OUT}(t) \cong \sum_{n=1}^{\infty} g_n[v_{IN}(t)]^n - \sum_{n=2}^{\infty} g_n[v_{IN}(t)]^n = g_1 v_{IN}(t) \tag{8}$$

which shows the perfect cancellation of nonlinearities of the overall transconductance amplifier in Fig. 3.

One can calculate THD for both original and linearized circuit assuming the transfer characteristic (3) for

all transconductors (in particular, we no longer neglect higher order terms in the output current of $G^{\langle 3\rangle}$ as in (8)). The results of numerical calculations are presented in Figs. 4, 5 and 6. Figure 4 shows theoretical THD characteristics for the considered circuits. Figures 5 and 6 show theoretical transfer and transconductance characteristics, respectively. It is worth noting that using the active-error feedforward technique one can obtain not only significant reduction of THD but also considerable increase of linear range of operation (recall that the transfer characteristic for differential pair transconductor saturates for $x \approx 0.7$; for linearized circuit it happens for $x \approx 1.2$).

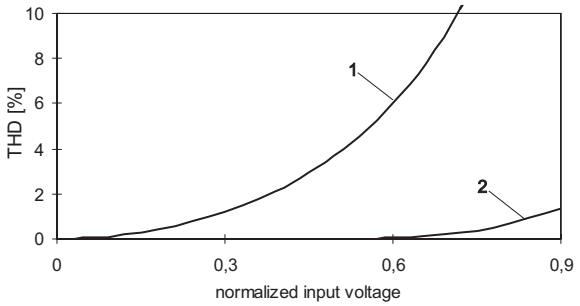

Fig. 4. Theoretical THD characteristics for (1) simple differential pair transconductor, (2) linearized transconductor

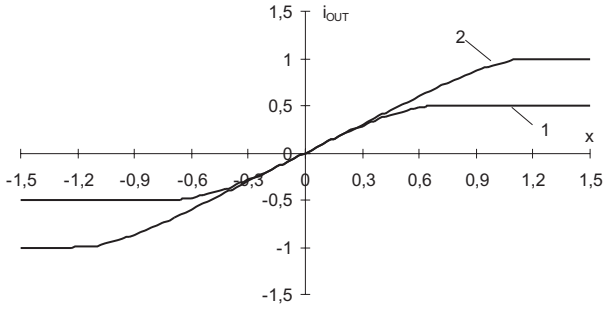

Fig. 5. Theoretical transfer characteristics for (1) simple differential pair transconductor, (2) linearized transconductor

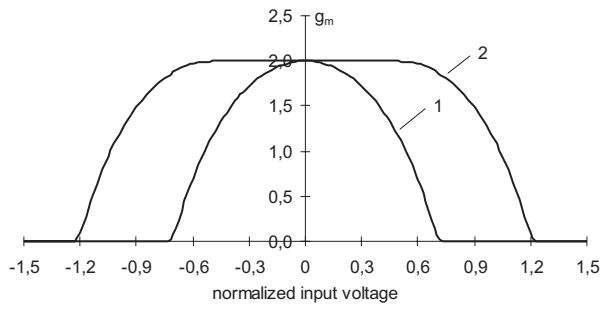

Fig. 6. Theoretical transconductance characteristics for (1) simple differential pair transconductor, (2) linearized transconductor

3. Frequency response of linearized OTA-C integrator

In this section, we shall consider the frequency response of the linearized transconductor. In order to get adequate results, we use the model of transconductor shown in Fig. 7. The OTA itself is treated as an ideal voltage-controlled current source of transconductance g_1. The rest of the elements in Fig. 7 are: C_i — input capacitance, C_o — output capacitance, C_c — coupling capacitance, g_o — output conductance.

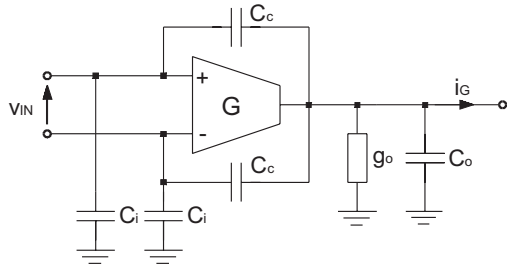

Fig. 7. Transconductor model including parasitic conductance and capacitors

It is commonly known in the literature (e.g. [4]) that the transfer function of differential pair transconductors exhibits a RHP zero which is formed due to feedforward path through gate-drain capacitance C_{gd}. In the structure in Fig. 7, this effect is modelled by capacitors C_c. This zero introduces excess phase lag at high frequencies, which can be the limiting factor in applications requiring a precise phase response, e.g. filters. Cancellation methods of RHP zeros can be found in the literature [21], [22]. As we will shown, RHP zero due to the capacitor C_c is cancelled in a natural way in the active-feedforward linearization structure in Fig. 3.

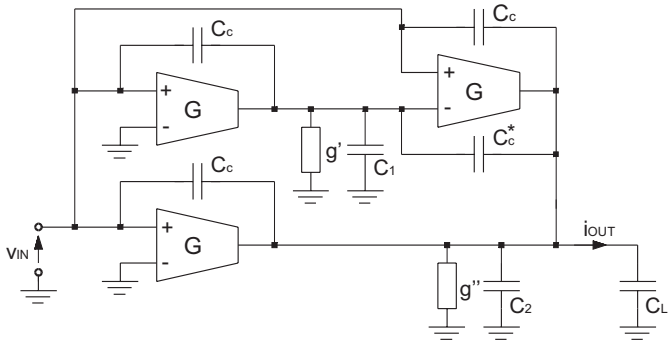

Fig. 8. Three-block feedforward transconductance amplifier with parasitic elements, working as an integrator loaded with capacitor C_L

Now, we apply the model in Fig. 7 to the feedforward transconductance amplifier in Fig. 3, which, together with the load capacitance C_L, forms the integrator presented in Fig. 8. We assume that all tranconductors are the same. The elements in Fig. 8 are: $g' = g_1 + g_o$, $g'' = 2g_o$, $C_1 = C_o + C_c + C_i$, $C_2 = 2C_o + C_c$. Capacitor C_c^* equals

C_c, however, it is distinguished for the reasons to be explained later.

The circuit in Fig. 8 is a two-zero and two-pole system. Both zeros and poles are real and negative. Its transfer function $H(s)$ can be easily calculated using the general G_m-C filter model [36]. The formula for $H(s)$ is the following

$$H(s) = H_0 \frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \tag{9}$$

where

$$H_0 = \frac{g_1}{2g_o}, \qquad \omega_{z1} = \frac{g_1}{C_c}, \qquad \omega_{z2} = \frac{g_1}{2C_1 + 3C_c^*} \tag{10}$$

and the poles can be approximated (on assumption $g_1 \gg g_o$) by the following formulas

$$\begin{aligned} \omega_{p1} &= \frac{2g_o}{C_L + C_2 + 2C_c^*}, \\ \omega_{p2} &= \frac{g_1}{C_1 + C_c^*(C_L + C_2 - C_1)/(C_L + C_2 + 2C_c^*)}. \end{aligned} \tag{11}$$

We observe that zeros are independent of the load capacitance C_L. For C_L much larger than the rest of the capacitances, which is usually the case, the above formulas can be approximated as

$$\omega_{p1} = \frac{2g_o}{C_L}, \qquad \omega_{p2} = \frac{g_1}{C_1 + C_c^*}. \tag{12}$$

Now, since $g_o \ll g_1$, it turns out that ω_{p1} is a dominant pole. Actually, it is a corner frequency of the integrator. Moreover, we have $\omega_{p1} < \omega_{z2} < \omega_{p2} \ll \omega_{z1}$ (the last inequality follows from the fact that $C_c \ll C_1$). It is seen that the frequency of ω_{z2} is slightly smaller than that of ω_{p2} (they differ by factor 2 to 3 depending on the relation between C_1 and C_c^*).

It is worth noting that there are no RHP zeros, so no cancellation is needed. In practical circuit implementations there are always additional poles (e.g. due to output current mirrors; see Fig. 9) which introduce phase lag. This excess phase can be compensated by capacitor C_c^*. To this end one has to increase C_c^* by connecting in parallel additional compensating capacitor. Note that this compensation scheme is simpler than the commonly used method [26], [27]. It follows that unlike the compensation scheme proposed in [16], the proposed circuit allows us to obtain very good linearity as well as compensation of the phase characteristic at the same time. This indicates the potential of the circuit for use in high-frequency filtering, where both features are of equal importance.

4. Linearized differential pair OTA implementation

In Fig. 9 a circuit implementation of the active-error feedforward linearization concept discussed in Section 3 is shown. The common mode feedback circuit (CMFB) is shown in Fig. 10. Note that the circuit in Fig. 9 is a differential-input two-output OTA, which follows from the fact that such a configuration is more suitable for filtering applications. Thus, it is a slight modification of the concept presented in Fig. 3. Transistors $Q_{1,2,7,8}$ form classical differential source-coupled pairs with current sink realized by transistor Q_{26}. Actually, the pair Q_1,Q_2 implements two-output counterpart of transconductor $G^{\langle 1\rangle}$ in Fig. 3. Transistors Q_7,Q_8 implement the counterpart of transconductor $G^{\langle 2\rangle}$ loaded by resistor $1/2g_m$. Differential pairs Q_3,Q_4 and Q_5,Q_6 with current sinks Q_{25} and Q_{27}, respectively, realize error amplifiers corresponding to $G^{\langle 3\rangle}$ in Fig. 3. The transconductors have common current sources realized by transistors $Q_{12–15,20,21}$ and $Q_{16–19,22,23}$. Note that in order to change the transconductance of the circuit in Fig.9, the bias current I_{bias} and resistor $1/2g_m$ have to be adjusted simultaneously.

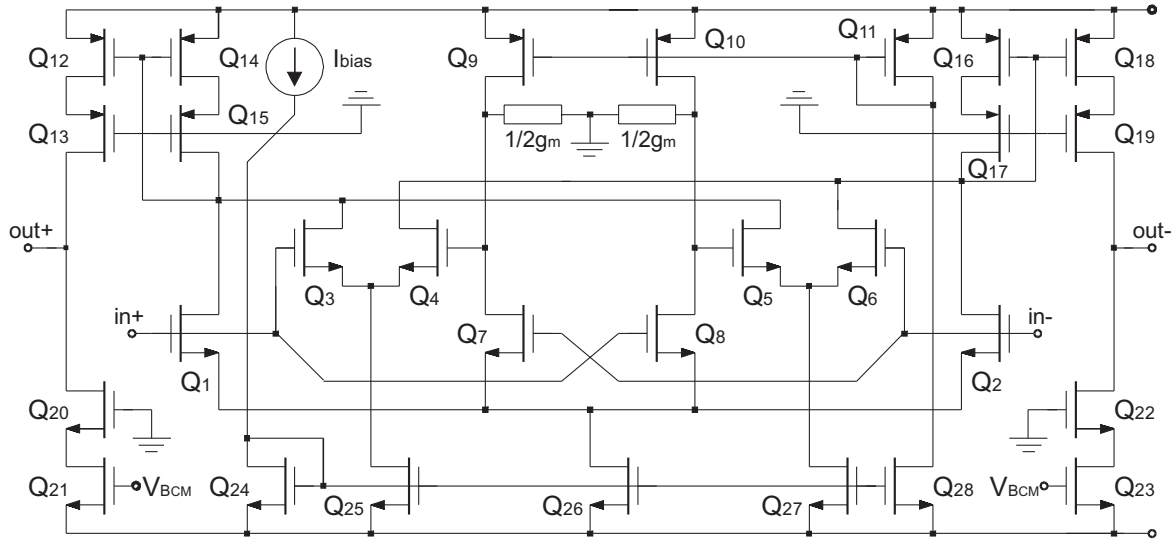

Fig. 9. Complete diagram of the linearized CMOS OTA

Phase compensation scheme

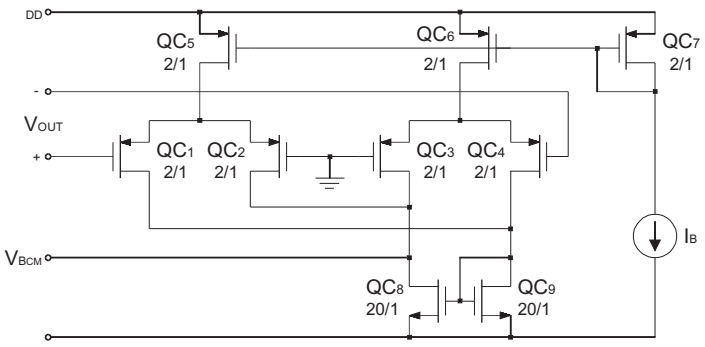

Fig. 10. Common-mode feedback circuit

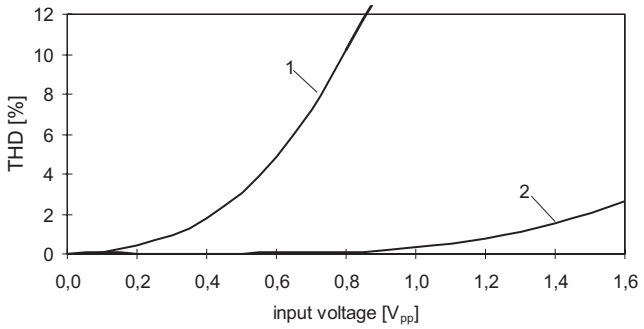

Fig. 12. SPICE simulated THD characteristics of the circuit in Fig. 9 with 1MHz sine wave: (1) without linearization, (2) with linearization

5. Simulation results

The complete circuit in Fig. 9 was designed for the 0.35-mm AMS process and simulated using SPICE. All p-channel and n-channel transistors have their bulks connected to V_{DD} and V_{SS}, respectively. The W/L ratios for transistors in Fig. 9 are: 4/1 for Q_{1-8}, 30/1 for $Q_{9-19,21,23-27}$, 60/1 for $Q_{20,22}$ and 15/1 for Q_{28}. Channel length is 1μm for all transistors. The bias current was set to $I_{bias} = 40$ μA. The circuit was simulated with $V_{DD} = -V_{SS} = 1.25$ V. The power consumption of the circuit is about 0.94 mW (including CMFB).

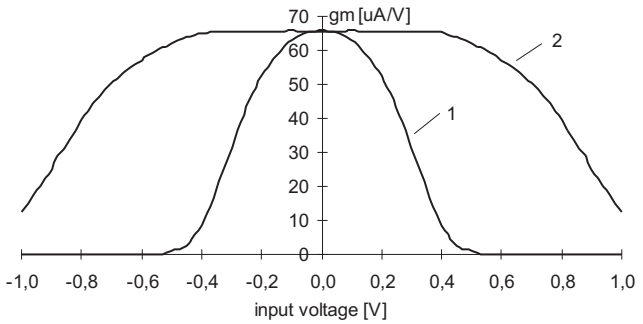

Fig. 11. SPICE simulated transconductrance characteristics of the circuit in Fig. 9: (1) without linearization, (2) with linearization

Figure 11 shows the simulated transconductance characteristic of the circuit in Fig. 9 and the reference simple differential pair transconductor in Fig. 2, respectively. It is seen that the improved linearity of overall transconductance element is obtained without deteriorating the transconductance of the circuit. This is not the case for the feedback technique, where the improvement of linearity is obtained at the expense of reduced transconductance of the overall element. Moreover, we can observe a significant increase of the linear input voltage range for the linearized circuit, which confirms the theoretical predictions presented in Section 3.

In order to have a quantitative measure of linearity improvement, the total harmonic distortion has been calculated for the circuit in Fig. 9 assuming 1 MHz sine wave input. The THD characteristics of the circuit with and without linearization are shown in Fig. 12. We can observe a big difference between both curves in Fig. 12. For example, THD at $0.8V_{pp}$ input signal for linearized circuit is less than 0.1% while THD for the circuit without linearization is about 10.2%. For input signal $1.2V_{pp}$ the figure is 0.78% and 21%, respectively. These results also confirm the theoretical predictions of Section 3.

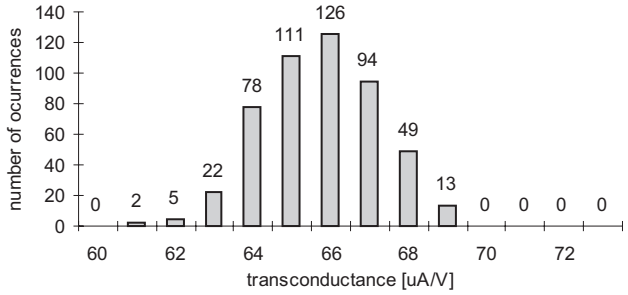

Fig. 13. Monte-Carlo simulation results for transconductance of OTA in Fig. 9 for $I_{bias} = 40\mu$A and 1% deviations (with gaussian distribution) in V_{th} and k

Monte-Carlo simulations have been performed in order to check how the transistor mismatch affects transconductance of OTA circuit. Figure 13 shows the Monte-Carlo simulation results for the transconductance of the OTA in Fig. 9. The simulations have been carried out assuming 1% deviation (with gaussian distribution) in V_{th} and transconductance parameters for all circuit transistors. A bias current has been set to 40 μA. The mean value of g_m is 65.7 μA/V, while the standard deviation of g_m is 1.5 μA/V.

It turns out that the OTA circuit in Fig. 9 has a very good tuning capability. Some of the data is shown in Table 1 as well as in Fig. 14. Recall that it is necessary to change both the bias current and the value of the reference resistors $1/2g_m$, while tuning the circuit.

Table 1
Tuning capability for the linearized OTA circuit in Fig.9

Ibias [μA]	g_m [μA/V]	Power consumption [μW]	DC gain [dB]	Ibias [μA]	g_m [μA/V]	Power consumption [μW]	DC gain [dB]
0.5	3.0	0.10	88.2	8.0	28.2	0.26	80.7
1.0	5.7	0.12	87.5	16.0	42.3	0.43	72.5
2.0	10.2	0.14	86.3	32.0	59.9	0.77	50.4
4.0	17.5	0.18	84.3	50.0	69.6	1.14	39.8

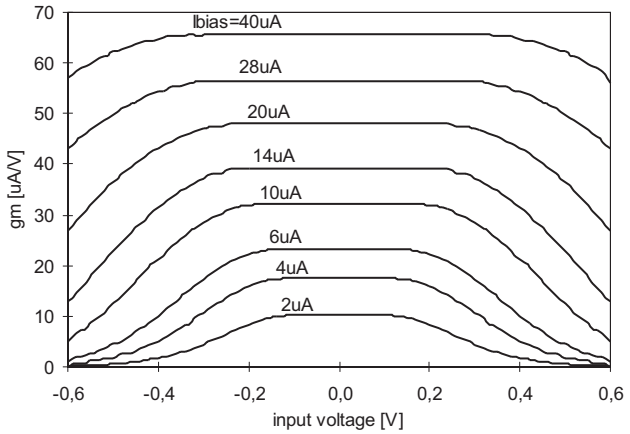

Fig. 14. Transconductance tuning capability for OTA in Fig. 9

In order to illustrate the performance of the compensation scheme introduced in Section 3, the OTA-C integrator with 1pF load has been simulated without and with phase compensation using two capacitors of 0.035 pF connected between resistors $1/2g_m$ and OTA outputs (I_{bias} = 20 μA). Figure 15 shows phase characteristics for the circuit in those two cases. It follows that the phase compensation allows us to significantly enlarge the frequency of 1° excess phase (the figure is 3.8 MHz and 63.5 MHz without and with compensation, respectively).

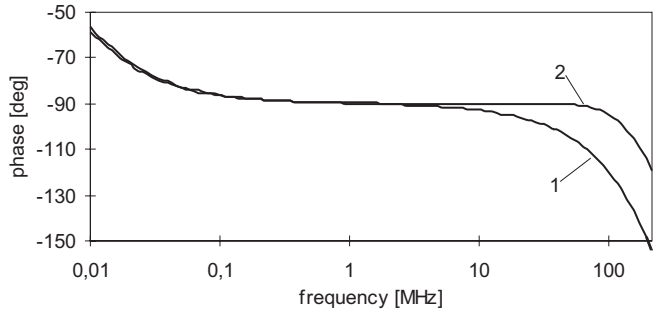

Fig. 15. Phase characteristic of OTA-C integrator with 1pF load (1) without phase compensation, (2) with 0.035pF compensation capacitor

Based on the simulation results, we can assert that the presented OTA circuit does not exhibit drawbacks mentioned in the introduction, which are common to the most of the linearization techniques described in the literature ([20–34]). Its main features are: no reduction of transconductance factor in comparison to the simple differential pair, significant increase of linear range of operation, high efficiency of linearization (i.e. large linear output current), very low power consumption, no RHP zeros, easy and effective phase compensation.

6. Filter example

In order to illustrate the robustness of both linearization scheme and phase compensation, a 3$^{\text{th}}$ order low-pass elliptic G$_m$-C filter in Leap-Frog (LF) structure with floating capacitor [37] has been designed and simulated. The general structure of the filter is shown in Fig. 16. We have assumed 10.0 MHz cut-off frequency, minimum pass-band gain 0.9, and maximum stop-band gain 0.16. Element values are: g = 60 μA/V (bias current equal to 32 μA), C_1 = 1.98 pF, C_2 = 1.06 pF, C_3 = 0.80 pF, C_4 = 1.60 pF.

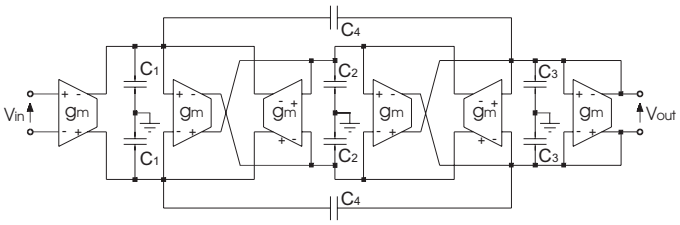

Fig. 16. Diagram of the 3$^{\text{th}}$ order low-pass elliptic G$_m$-C filter in LF structure with floating capacitor

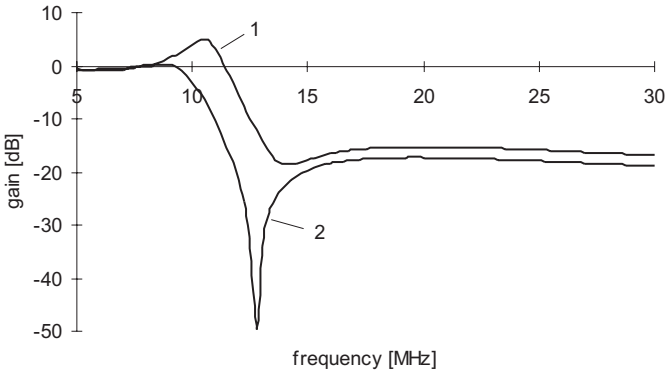

Fig. 17. Amplitude characteristic of 3$^{\text{rd}}$ order elliptic filter in Fig. 16: (1) without phase compensation, (2) with phase compensation of OTA

Figure 17 shows the amplitude characteristics of the filter. In the first case, the filter was simulated assuming transconductors without phase compensation. We can observe that its transfer function exhibits large distortions. While using compensated OTAs (compensating capacitors equal to 0.054 pF), characteristic of the filter is almost ideal, especially the quality of the transfer function zero is excellent.

We have also tested linearity of the overall filter. For the sake of comparison we have considered two cases. In the first one we have simulated the filter with conventional differential pair transconductors in Fig. 2. It follows that THD of the output signal of the filter with 1 MHz sine wave input equals 4.1% (14.3%) for $0.6V_{pp}$ ($1.0V_{pp}$) input signal amplitude. The filter in Fig. 16 has been also implemented using linearized transconductors in Fig. 9. The simulation results for the filter with linearized OTAs show that THD of its output signal with 1 MHz sine wave input equals 0.1% (0.28%) for $0.6V_{pp}$ ($1.0V_{pp}$) input signal amplitude. Thus, application of linearized transconductors gives a significant reduction of the nonlinearity distortion of the whole filter circuit. Due to the increase of the linear input voltage range of the circuit in Fig. 9, the filter can now work with much larger input signals. For example, THD level of 1.0%, which was obtained for the filter with reference differential pair transconductors with $0.4V_{pp}$ of input signal, is now attained for input signal amplitude equal to $1.2V_{pp}$.

7. Conclusions

An effective linearization method based on the active-error feedforward concept has been developed for realizing a very linear CMOS OTA. The proposed circuit technique combines a classical source-coupled differential pair transconductor with a simple error amplifier in feedforward path. Theoretical considerations have been performed using power series expansion of the transfer characteristic of differential pair transconductor. The complete linearized OTA in differential-input two-output structure has been simulated via SPICE using the 0.35-μm AMS process. For power supply $\pm$1.25 V, total harmonic distortion at $0.8V_{pp}$ is less than 0.1%. The circuit has very low power consumption, which is less than 1mW for the bias current equal to 40 μA. The obtained simulation results confirm that the linearity of the overall transconductance element is significantly improved in comparison to the reference circuit (i.e. simple differential pair transconductor). Moreover, a significant increase of the linear input voltage range for the linearized circuit was observed. The efficient phase compensation can be applied, which makes the circuit suitable for high-frequency filtering. It is worth noting that the compensation scheme follows directly from that linearized circuit topology and requires no additional circuitry except one capacitor.

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