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Reliable digital dead-time generator for the GaN HEMTs based H-bridge converters

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Abstract: The paper deals with hardware solution of a fully digital dead-time generator. The circuit is applicable to the H-bridges based on any type of semiconductor switching devices including SiC, IGBT, Si-MOSFET and up-to-date GaN HEMTs. The generation of dead-times is ensured by commercially available silicon delay lines. High temperature stability is obtained by self-compensation of propagation delay of logic elements thanks to the symmetry of design topology. The circuit can be set-up to generate dead-times in the range from 10 ns to 500 ns. Longer dead-times are also available by simple cascading of the silicon delay lines. The key motivation for development of the circuit was unavailability of ready to use integrated solutions on the market. Moreover, contrary to the other solutions the proposed circuit is immune to prospective oscillations of an input PWM signal. The paper brings a detailed analysis of the circuit principle, results of the verification of a sample solution and an example of practical application as well.

Key words: dead-time generator, delay-line, GaN HEMTs, H-bridge driver

1. Introduction

The H-bridge configuration of power elements is widely used in the implementation of various converters, class-D amplifiers and other appliances. The direction of the load current is controlled in the configuration by simultaneous switching of diagonal elements of the H-bridge. Switching devices i.e. silicon metal-oxide-semiconductor field-effect transistors (Si-MOSFETs), insulated gate bipolar transistors (IGBTs), silicon-carbide transistors (SiCs) and gallium-nitride high-electron-mobility transistors (GaN HEMTs) are usually driven by specialized drivers. The drivers are controlled by a complementary pair of pulse width modulation (PWM) signals that determine switching of particular power elements. To let the power stage work properly and

efficiently there also must be implemented a dead-time generator circuit. Its goal is to prevent the power stage form temporary short of power supply caused by the simultaneous switch of improper high and low elements during the PWM signal transitions.

Wrong arrangement or failure of the dead-time circuit can lead to superfluous overheating of the power stage or even damage of the H-bridge due to shoot-through. Thus, appropriate design and set-up of the dead-time generator is essential [1, 2]. Generally, the use of modern high speed switching devices requires a precise and temperature independent dead-time generator to be implemented.

Most of up-to-date driving ICs incorporate a properly adjusted dead-time generator. On the other hand, the driver ICs with no implemented dead-time circuit are available as well. The up-to-date half bridge drivers LM5113 [3], LMG1205 [4] or LMG5200 [5] can be mentioned here as the examples of ICs with no inner dead-time circuits. When the ICs are used it is necessary to implement the dead-time generator externally. This brings a possibility to set and adjust the dead-time in accordance with the needs of application and the requirements of a designer.

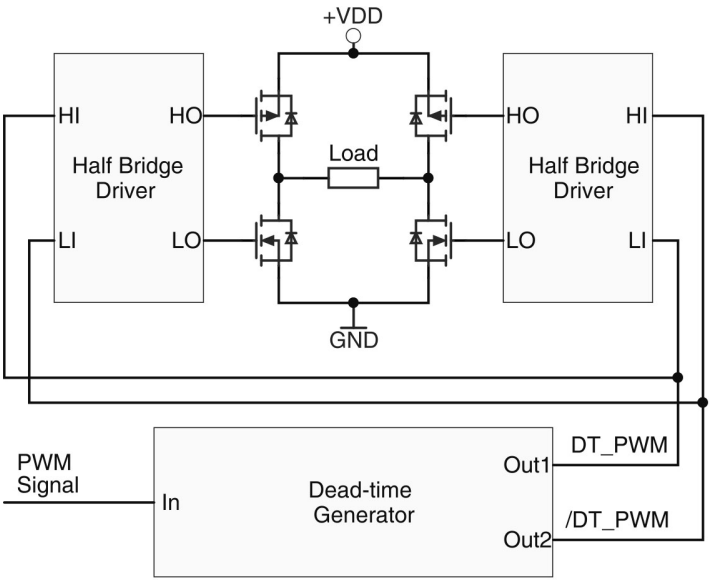


Fig. 1. H-bridge controlled by the PWM signal

2. Conventional fixed dead-time generator

A typical conventional dead-time generator is presented in Fig. 2(a) [6, 7]. The PWM input represents the signal coming from the pulse width modulator. Dead-time pulse-width modulation outputs (DT_PWM and /DT_PWM) drive particular pairs of power transistors of the H-bridge. The length of the dead-time is determined by a delay circuit.

Most simply, the delay circuit can be based on the RC network [8–10]. Thus, a relatively wide range of delay times including an ns margin can be achieved. However, this approach suffers

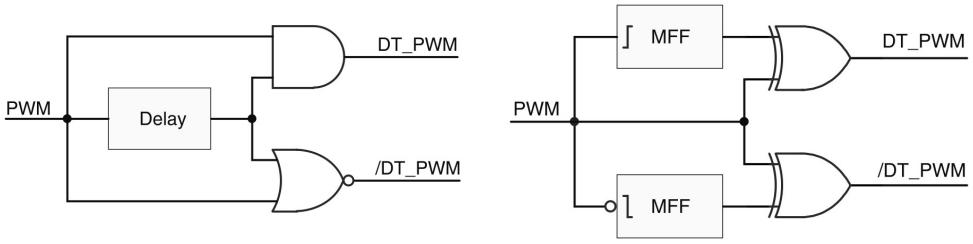


Fig. 2. Conventional dead-time generator topologies: using a delay circuit (a); using the monostable flip-flops (b)

from certain drawbacks. Primarily, the RC networks and the gates demonstrate high temperature dependence. Secondly, the adjustment of the dead-time must be done manually and individually. Finally, the repeatability of the circuit is questionable. The propagation delay of the chain of several logic gates can be employed here to create the delay line too. Unfortunately, in such a case the precise dead-time adjustment is not possible and the temperature dependence can be enormous. Logic gates are usually specified by typical and maximum propagation delay at room temperature. The span is not negligible. For example, in the case of SN74LV00A the data sheet defines 4.9 ns of typical and 7.5 of maximum value of propagation delay @ 25°C. Within the permitted operating temperature range of SN74LV00A the expected span is even much higher (from 1 ns to 8.5 ns for −40°C to 85°C) according to data sheet specification.

The delay can be generated using monostable flip-flops (MFF) in an appropriate topology [11, 12] as well, see Fig. 2(b). Popular timers are 74123, 555, etc. Apart from this, there is also a possibility to use a programmable one-shot generator (e.g. LTC6993). Unfortunately, the use of the commercially available integrated MFF or one-shot generators brings troubles with the lower margin of the generated time periods. Generally, the circuits mentioned above are well tailored to generate pulses of width within a 100 ns range or longer. Generation of shorter pulses is conditioned by the use of external timing components close to technical limits and at margins of application curves of the ICs. For example, in the case of SN74LV123 (dual monostable multivibrator) the timing is set by an external resistor and capacitor. The shorter the output pulse has to be the lower both of the component values must be set. In accordance with the application curves (see the SN74LV123 data sheet) the 60 ns pulse can be theoretically achieved using $R_{\text{ext}} = 1\ \text{k}\Omega$ (absolute minimum value) and $C_{\text{ext}} = 10\ \text{pF}$. It is evident that a precise set of the external capacity to 10 pF can be an issue as the parasitic capacitances of the PCB layout of the same order can be expected. Moreover, the switching characteristics of SN74LV123 reveal much higher variation of narrow pulses than the wide ones. The NE555 timer IC seems to be even more unsuitable. In compliance with the NE555 data sheet the typical output pulse rise-time at room temperature is 100 ns. Moreover, the maximum rise-time can be 2 or 3 times longer. As the parameter is similar for the output pulse fall-time, it is clear that generation of pulses shorter than several μs is practically impossible. In the case of LTC6993 the IC is strictly defined as a one-shot pulse generator of pulses within the range from 1 μs to 33.6 s (see the LTC6993 data sheet). This limits the use of the mentioned circuits. They can be

applied in converters with switching frequency up to several tens of kHz at maximum. The use of traditional Si-MOSFETs is meaningful in this range. However, as for the converters equipped with GaN HEMTs the solution is inappropriate, as it diminishes the benefits of the high speed devices.

Regardless the kind of delay circuit, the topologies in Fig. 2 are not immune to prospective oscillations of the input PWM signal or short glitches at all. The problem can arise in the case of the occurrence of unwanted oscillations of the PWM signal due to the presence of noise or misbehavior of the modulator. Provided the oscillations period is shorter than the delay of the delay circuit, the dead-time will not be generated properly and reliably.

3. The proposed circuit

Unlike the above mentioned solutions, there is presented a novel dead-time generator combining logic gates, flip-flops and silicon delay lines to achieve more temperature invariant design. In comparison to the conventional solutions the delay is not generated by chain of gates but by specialized ICs. The used silicon delay line demonstrates much lower temperature variation than the chain of logic gates. In accordance with DS1100 data sheet specifications [13] the maximum delay variation is only ±13% within the industrial temperature range (−40°C to 85°C). To the contrary, for SN74LV00 NAND gates the typical propagation delay is 4.9 ns (measured @ 25°C) and it can vary from 1 ns to 8.5 ns within the industrial temperature range. This translates to approximately ±80% variation for the chain of gates based on SN74LV00 ICs. Moreover, the two-stage flip-flop solution ensures the immunity of the circuit to prospective oscillations of the PWM signal.

The input of the circuit is at TP1. The XOR gates (IC1A, IC1B) generate a pair of complementary signals. As both XOR gates are subjects of the same package there can be expected approximately the same propagation delay and the same temperature dependence too. The input signal is duplicated at TP2 and, simultaneously, inverted at TP3. These signals are led to the D-flip-flops (IC2A, IC5B). The front edge of TP2 signal sets the IC2A latch. TP4 turns to H and TP5 to L at the same time. This activates and sets the next D-flip-flop (IC5A). There can be found the H level (TP7) and L level (TP5) at the input of the AND gate (IC6A) at the moment. The output of the AND gate (TP8) is in L. The propagation delay of IC5A plays a vital role here as it ensures that the signal TP7 is always delayed to TP5. The moment of transition of the signal TP8 from L to H is principally defined by the IC3 delay line, DS1100. At the moment the L level appears at the output of the delay line IC3 (TP6), there comes reset of the IC2A latch and TP5 goes high. By this mechanism the DT_PWM signal at the output of the IC6A gate goes high as well. At the same time the IC2B latch comes to reset. The DT_PWM stays H until IC5A is cleared by the /CLR input. Zeroing of IC5A is done at the moment when the rear edge of the input PWM signal affects the IC1B invertor and sets the IC5B D-flip-flop (TP10 goes low).

The circuit is symmetrical for both the signal lines (DT_PWM, /DT_PWM). That is why the section for generation of the complementary signal /DT_PWM works the same way. The fundamental feature of the circuit is the safe start point. An occurrence of any edge of the input signal (no matter whether front or rear one) triggers the zeroing of both complementary outputs. The dead-time is always subtracted from the width of a prospective PWM pulse. The principle of

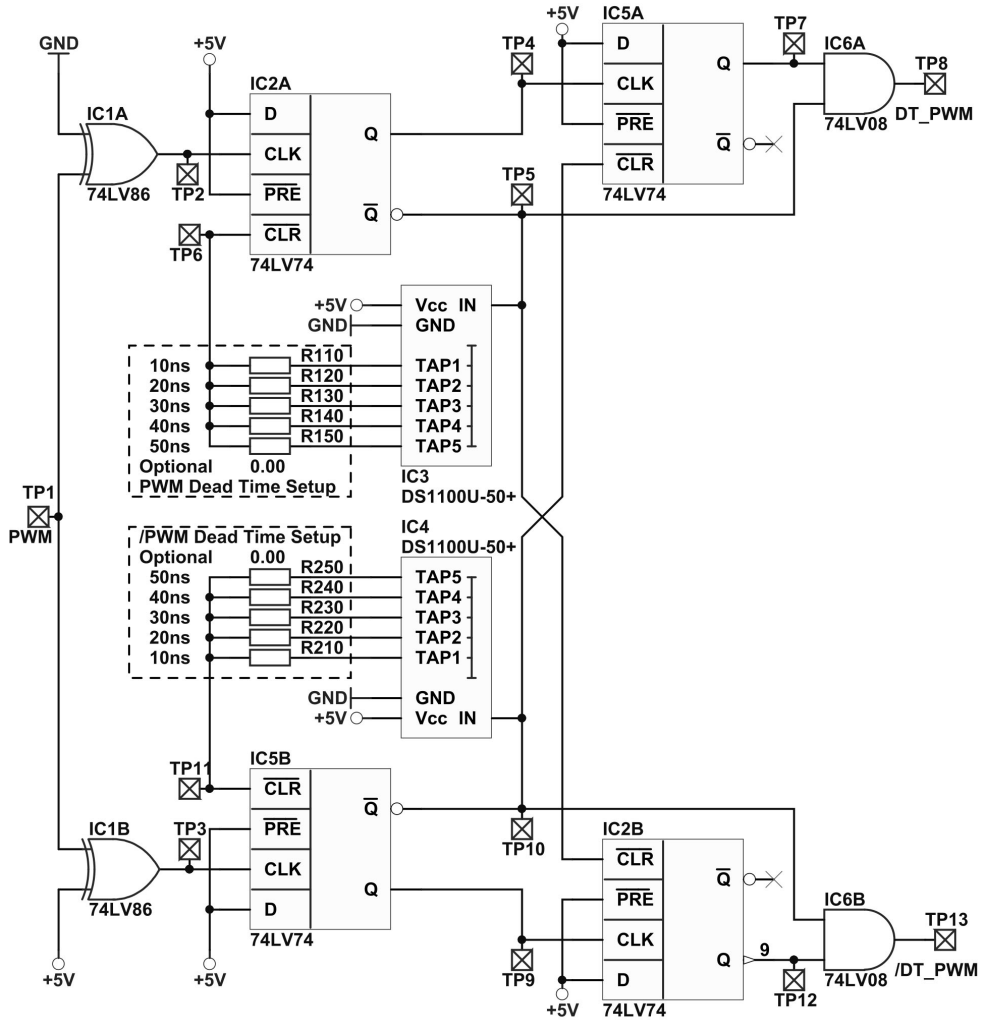


Fig. 3. The proposed circuit of the dead-time generator

the circuit and its functionality is clear from the time chart in Fig. 4. The chart reflects propagation delays of particular gates and latches of the circuit. The relevant periods in the event of occurrence of the rear edge of the PWM signal are indicated here.

Obviously, the propagation delays of particular elements of the circuit are affected by thermal drift. This phenomenon is partially compensated by topology of the circuit and appropriate arrangement of the elements to common packages (IC1A-IC1B, IC2A-IC2B, IC5A-IC5B, IC6A-IC6B). The dead-time is determined by the time difference of T_A and T_B periods. T_A is defined as a period between arrival of the rear edge of the PWM signal and the set-up of the /DT_PWM signal to H. T_B is defined as a period from arrival of the rear edge of the PWM signal to zeroing of

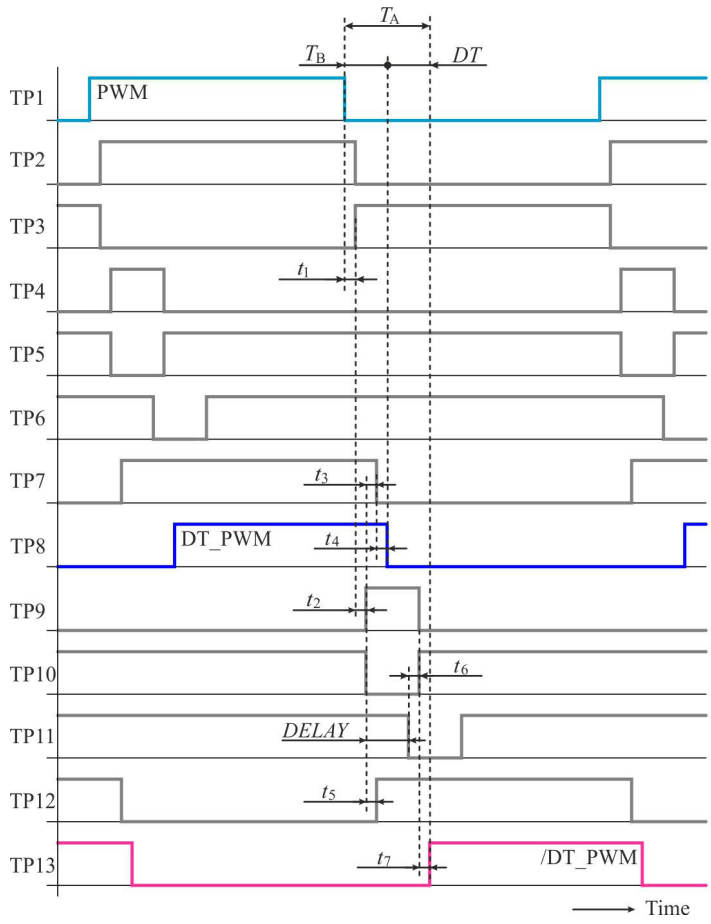


Fig. 4. Time chart of the proposed dead-time circuit for rear edge of the PWM signal occurrence (the waveforms relate to particular test-points denoted in Fig. 3)

the DT_PWM output. The T_A period is affected by the delay line IC4 (*DELAY*) and propagation delays of corresponding logic elements (t_1, t_2, t_6, t_7). The T_B period is determined by t_1, t_2, t_3, t_4 propagation delays only. The meaning of these particular periods is explained in Table 1. The resulting dead-time is

$$DT = T_A - T_B = t_1 + t_2 + DELAY + t_6 + t_7 - (t_1 + t_2 + t_3 + t_4) = DELAY. \tag{1}$$

As the propagation delays t_6, t_3 arise on elements of the same type and as these elements are located in the same package (see Table 1), it can be expected that t_6, t_3 values will be very close to each other. Due to the opposite signs, see (1), these periods eliminate each other. The same it is with t_7 and t_4 values. Moreover, it can be expected that the prospective thermal drift of propagation delays of the elements will be mutually compensated as well.

Table 1. Typical propagation delays of particular logic elements used in the circuit design (data sheet values by Texas Instruments Inc.)

Period symbol	**IC**	**Signal direction**	**Package**	**Propagation delay, typ. (ns) @ 25°C**
t_1	SN74LV86A	In→Out	IC1B	3.7
t_2	SN74LV74A	CLK→Q resp. CLK→/Q	IC5B	5.6
t_3	SN74LV74A	/CLR→Q resp. /CLR→/Q	IC5A	5.0
t_4	SN74LV08A	In→Out	IC6A	4.1
t_5	SN74LV74A	CLK→Q resp. CLK→/Q	IC2B	5.6
t_6	SN74LV74A	/CLR→Q resp. /CLR→/Q	IC5B	5.0
t_7	SN74LV08A	In→Out	IC6B	4.1
DELAY	DS1100	In→Out	IC4	20

The main advantage of the solution is the immunity to the short pulses and oscillations at the PWM input. In the case of an occurrence of oscillations within a period shorter than the delay of the delay lines, the outputs DT_PWM and /DT_PWM are guaranteed to stay safely at the L level.

4. Implementation and verification

The dead-time generator was successfully tested and applied in the design of a power converter for driving of electro-dynamic actuators similar to a vibration test bench, see Fig. 5. The core of the converter is based on an analogue PWM modulator running at 600 kHz. The rectangular output of the modulator controls the power stage formed by four GaN HEMTs (GS61008P). The transistors are configured in the H-bridge. The bridge is driven by two LM5113 drivers (each one dedicated to the half of the H-bridge). In accordance with recommendations of the transistors manufacturer, the delay lines were set-up to 20 ns (optional resistors R_{120}, R_{220} were mounted to activate the relevant tap outputs, see Fig. 3.

Signal waveforms measured at the input and output terminals of the dead-time generator for the case of the 50% duty cycle of the PWM signal are depicted in Fig. 6. The cyan waveform represents the output of the PWM modulator which is connected to the input of the dead-time generator. The blue and magenta waveforms are the complementary outputs of the dead-time generator (DT_PWM, /DT_PWM) used for direct cross driving of LM5113 ICs.

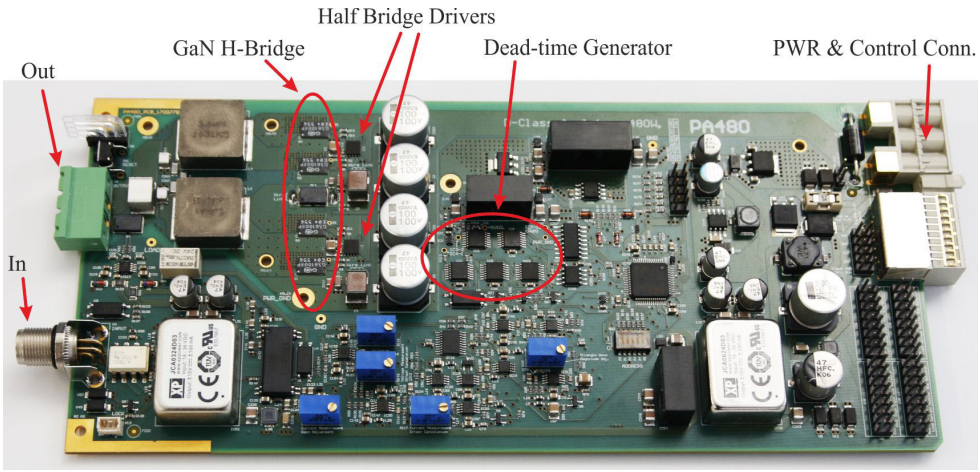
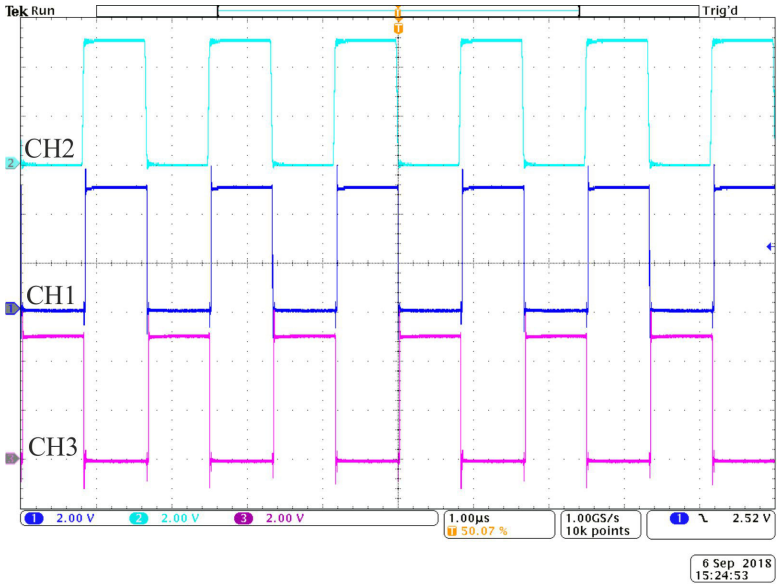


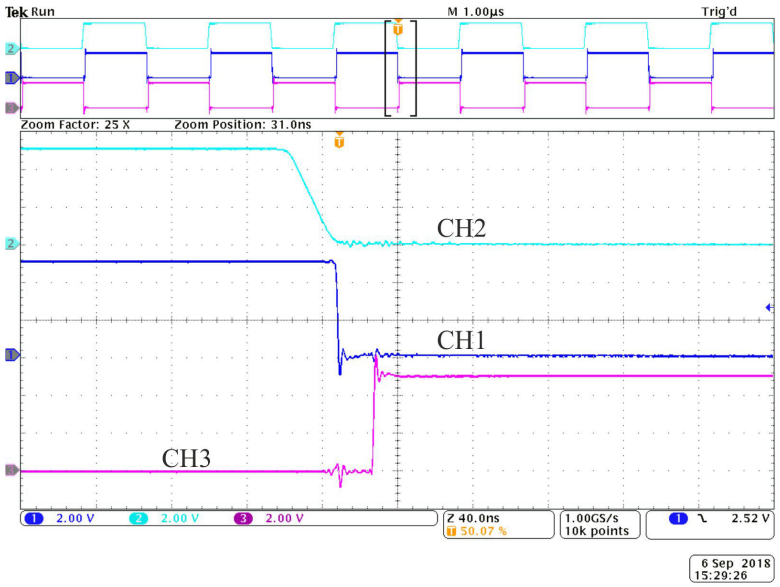
Fig. 5. The prototype of the 0.5 kW power converter with implemented dead-time generator (delay lines DS1100U-50+ and banks of the setting resistors are positioned on the bottom layer)

In addition to the basic functionality, the thermal stability of the design was tested as well. The measurement in a climatic chamber was done. As the minimal cable length to get the signals from the climatic chamber is around 1 m, there was necessary to place the oscilloscope probe tips inside the chamber alongside with the device under test (DUT). Using the simple coaxial cables to arrange the extended output lines was rejected. The arrangement would definitely lead to deterioration of the whole measurement due to excessive capacitive loading. For instance, the standard RG58 coaxial cable demonstrates a nominal capacity of 100 pF/m typically. To the contrary, the used 10:1 oscilloscope probes (TPP500B by Tektronix) demonstrate less than 4 pF of capacitive loading. Before the use the probes were properly frequency compensated and equipped with needed accessory for high speed measurements. The hook tips were dismounted. The alligator ground links were replaced by short ground springs to minimize the additional spurious inductance. The prepared probes were connected to the DUT. The whole arrangement was located in the climatic chamber and tested for the thermal span from −40°C up to +80°C with 10°C steps. After setting-up the desired temperature and necessary warm-up period, the measurement of both the dead-times DT_1 and DT_2 was done. DT_1 is the time from the rear edge of the DT_PWM to the front edge of /DT_PWM. DT_2 denotes time from the rear edge of the /DT_PWM to the front edge of DT_PWM. The measurement was done by a Tektronix MSO4105B oscilloscope.

Theoretically, the enormous temperature span used to test the DUT can impact the performance of the probes as well. Due to the temperature changes inside the chamber the division ratio and frequency compensation of the probes can be affected. On the other hand, as there was used a pair of identical probes for both outputs, the prospective changes can be expected more or less similar. The measured dead-time period is obtained as a difference between the times measured by the particular probes. Thus the prospective temperature drifts can be considered mutually compensated. Moreover, there was observed no visible deterioration of the signal shape during the thermal test (no amplitude changes, no steepness change of the edges).



(a)

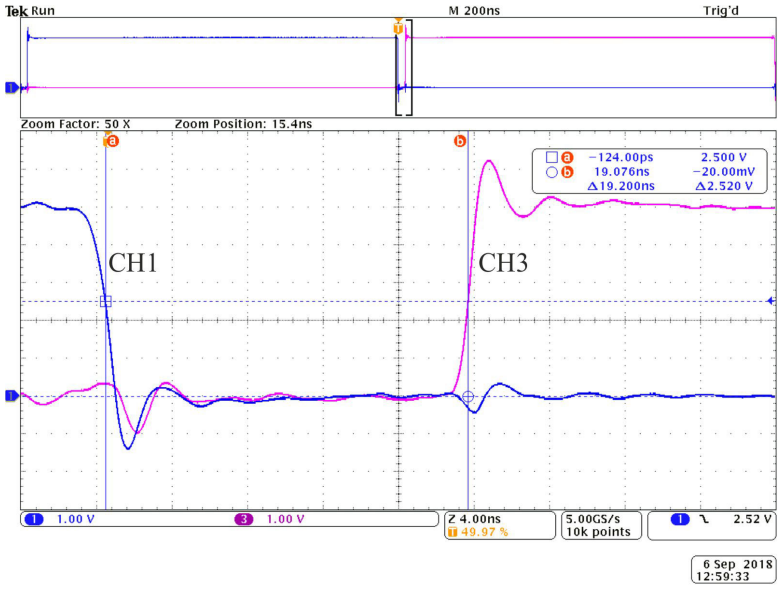


(b)

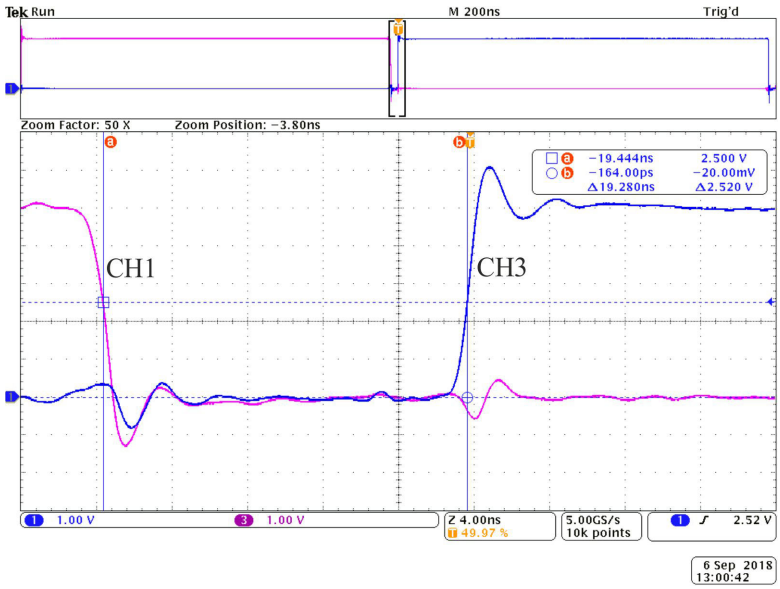
Fig. 6. Signals measured at the inputs and outputs of the dead-time generator – PWM = 600 kHz, 50% DCY, oscilloscope: CH1 – DT_PWM (blue), CH2 – PWM (cyan), CH3 – /DT_PWM (magenta), wide sweep-time view (a); PWM falling edge detail (b)

The DT_1 and DT_2 periods were measured for crossing the 50% level of nominal H value of the signals, see Fig. 7. The measured temperature dependence of both periods is depicted in

Fig. 8. In the case of DT_1 the average drift is less than 1.3 ps/°C. In the case of DT_2 it is even less than 1.2 ps/°C.



(a)



(b)

Fig. 7. Measurement of the temperature fluctuation of the dead-time periods – PWM = 600 kHz, 50% DCY, oscilloscope: CH1 – DT_PWM (blue), CH3 – /DT_PWM (magenta), measurement of DT_1 period (a); measurement of DT_2 period (b)

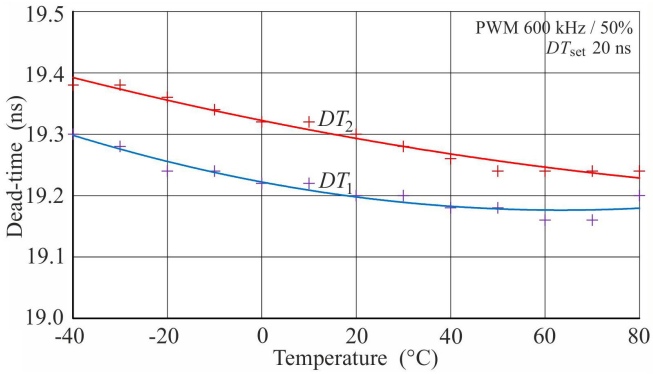


Fig. 8. Thermal stability of the dead time generator for dead-time set to 20 ns: blue – DT_1 thermal drift, red – DT_2 thermal drift, (points – measured values, curves – interpolation)

5. Conclusions

There was proposed and presented a new topology of a safe, temperature stable and oscillation resistant dead-time generator. The generator was successfully implemented into the power convertor with the output stage based on GaN HEMTs. The symmetry of the topology ensures mutual compensation of thermal effects. The resultant thermal dependence of dead-time is very low. The measured value of the temperature coefficient is 1.3 ps/°C within the temperature range from −40°C up to 80°C. Currently, the generator enables to set-up the dead-times from 10 ns up to 50 ns. With respect to the high/low side delay skew of the driver ICs it is an appropriate range for the GaN elements. In the case of necessity, there is possible to enlarge the dead-time as needed to tailor the dead-time generator for other switching devices. Demanded dead-time can be easily reached by substitution of the present delay lines for more suitable ones. With the DS1100 family the delays from 10 ns up to 500 ns are available. As the DS1100 circuits are equipped with several tap lines, there is theoretically possible to modify the delays by switching the tap lines and optimize the dead-time by means of feedback control during the operation.

Acknowledgements

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