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# Fault diagnosis of T-type three-level inverter based on bridge voltages

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**Abstract:** Multilevel inverters have been widely used in various occasions due to their advantages such as low harmonic content of the output waveform. However, because multilevel inverters use a large number of devices, the possibility of circuit failure is also higher than that of traditional inverters. A T-type three-level inverter is taken as the research object, and a diagnostic study is performed on the open-circuit fault of insulated gate bipolar transistor (IGBT) devices in the inverter. Firstly, the change of the current path in the inverter when an open-circuit fault of the device occurred, and the effect on the circuit switching states and the bridge voltages were analyzed. Then comprehensively considered the bridge voltages, and proposed a fault diagnosis method for a T-type three-level inverter based on specific fault diagnosis signals. Finally, the simulation verification was performed. The simulation results prove that the proposed method can accurately locate the open-circuit fault of the inverter device, and has the advantage of being easy to implement.

**Key words:** bridge voltage, fault diagnosis, fault signal, open-circuit fault, T-type three-level inverter

## 1. Introduction

Compared with traditional two-level inverters, multilevel inverters have been widely used in medium-voltage and high-power applications for the advantages of lower  $dv/dt$ , total harmonic distortion and so on [1–4]. In recent years, multilevel inverters have begun to be applied in some low-voltage situations [5, 6]. Hence, a T-type three-level inverter has been getting more and more attention because it is high-efficiency and has the characteristics of being suitable for low-voltage [7, 8]. However, there are a large number of power devices in one multilevel inverter.



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As a result, increasing the number of devices would not only increase the cost but also reduce the reliability of the inverter, as a break in any of these devices will inevitably make the entire system fail to work. Therefore, the fault diagnosis methods would be necessary to ensure the reliability of the multilevel inverter.

In literature [9], a fault diagnosis method was proposed to diagnose multiple transistor open-circuit faults in a T-type three-level inverter. In the paper, a finite-state machine (FSM) tracking state transitions and rough set theory (RST) were employed to distinguish state transitions under various fault modes. A diagnosis method of an open-circuit fault and fault-tolerant control strategy for T-type three-level inverter systems was proposed and the location of the faulty device can be identified by the average of the normalized phase current and the change of the neutral-point voltage [10]. Reference [11] conducted an open-circuit fault diagnosis study of the T-type three-level inverter device by detecting the midpoint current of the bus, the circuit state vector and the phase current polarity. Reference [12] carried out fault diagnosis research on the T-type three-level inverter by sampling the three-phase voltage of the inverter and adopting the error analysis method of the positive sequence, negative sequence and zero sequence voltage of the inverter. In order to simplify the diagnosis process, in view of the common electrical faults in the T-type three-level inverter fed by a dual three-phase permanent magnet synchronous motor driver, Reference [13] proposed a two-step diagnosis scheme. The first step was to determine the fault phase and fault category by analyzing the current trajectory on the harmonic subspace, and the second step was to determine the specific type of fault. However, most of the current fault diagnosis methods for T-type three-level inverters have a common feature that in the diagnosis processing one phase follows another. That is to say, a fault in the a-phase is diagnosed according to the fault characteristic signal of the a-phase. There are few methods that use certain fault characteristic signals to perform unified diagnosis on all the three-phase inverter devices.

In this paper a fault diagnosis method is proposed for the T-type three-level inverter. This method is based on a specific fault characteristic signal calculated from bridge voltages and it can realize unified fault diagnosis for all three-phase devices of the inverter. The second section briefly introduces the T-type three-level inverter and analyzes the effect of the open-circuit failure of the device on the inverter. The third section proposes specific fault diagnosis methods. The fourth section carries out simulation verification and the fifth section gives the conclusion.

## 2. Fault analysis of T-type three-level inverter

### 2.1. T-type three-level inverter

The topology of the T-type three-level inverter is shown in Fig. 1. This topology combines the advantages of traditional two-level inverters (low conduction loss, simple working principle, etc.) with the advantages of multi-level inverters [14]. In a T-type three-level inverter, the power devices  $S_{x1}/D_{x1}$  ( $x = a, b, c$ ) are called high-side devices and the power devices  $S_{x4}/D_{x4}$  are called low-side devices. These devices must withstand the entire input bus voltage  $V_{dc}$  like a traditional two-level inverter. The remaining power devices ( $S_{x2}/D_{x2}$  and  $S_{x3}/D_{x3}$ ) are called bidirectional devices and only need to bear half of the bus voltage. Here, the voltage between the bridge midpoint ( $a, b, c$ ) and the midpoint ( $o$ ) of the DC voltage of each phase is defined as the bridge voltage ( $v_{xo}$ ,  $x = a, b, c$ ).

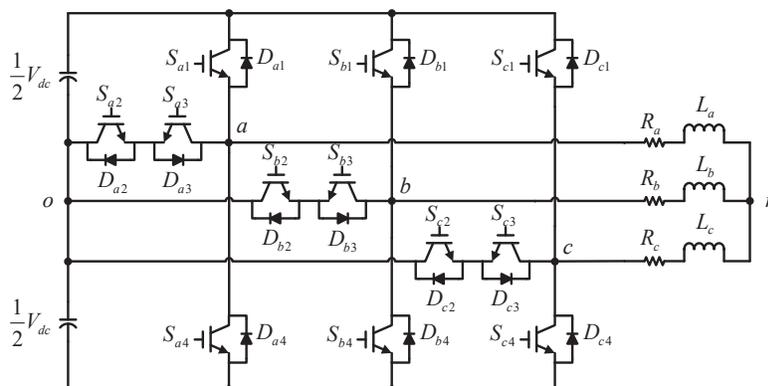


Fig. 1. Schematic of the T-type three-level inverter topology

A common control strategy for T-type three-level inverters [14, 15] is shown in Table 1. In the table, the switching command “1” indicates that the corresponding device is turned on, and the switching command “0” indicates that the corresponding device is turned off. The switching state “P” is realized by controlling  $S_{x1}$  and  $S_{x2}$  to be turned on, “Z” is realized by turning on  $S_{x2}$  and  $S_{x3}$  and “N” is realized by turning on  $S_{x3}$  and  $S_{x4}$  at the same time.

Table 1. Switching state, switching command and bridge voltage of the inverter

Switching state	Switching command ( $x = a, b, c$ )				Bridge voltage $v_{xo}$
	$S_{x1}$	$S_{x2}$	$S_{x3}$	$S_{x4}$	
P	1	1	0	0	$+V_{dc}/2$
Z	0	1	1	0	0
N	0	0	1	1	$-V_{dc}/2$

## 2.2. Fault analysis

If there is an open-circuit fault occurring in the devices of the inverter, the current path and the voltage waveform of the inverter will be affected and resulting in abnormal circuit operation. Here we take the devices in the a-phase as examples to analyze the influence of the open-circuit faults.

When an open-circuit fault occurs in  $S_{a1}$ , it can be seen from Table 1 that it may affect the switching state P. When an open-circuit fault occurs in  $S_{a2}$ , it may affect the switching states P and Z. When an open-circuit fault occurs in  $S_{a3}$ , it may affect the states Z and N. When an open-circuit fault occurs in  $S_{a4}$ , it may affect the state N. The detailed analysis is carried out according to different phase current directions in following.

When the phase current  $i_a > 0$  (taking the current direction shown in Fig. 2 as the reference direction), Fig. 2 shows the change of the phase current path before and after the open-circuit fault occurs in three different switching states. In the switching state P, the phase current flows through  $S_{a1}$  to the load in normal condition. It can be seen that only the open-circuit fault of  $S_{a1}$  will affect this state. When the open-circuit fault of  $S_{a1}$  occurs, the phase current will continue to flow through  $S_{a2}$  and  $D_{a3}$  as shown in Fig. 2(a). In the switching state Z, it can be seen that only the open-circuit fault of  $S_{a2}$  will affect the state of the inverter. After the open-circuit fault of  $S_{a2}$  occurs, the phase current will continue to flow through  $D_{a4}$ , as shown in Fig. 2(b). In the switching state N, the phase current flows through  $D_{a4}$  under normal conditions, so an open-circuit fault of any device will not affect this state as shown in Fig. 2(c).

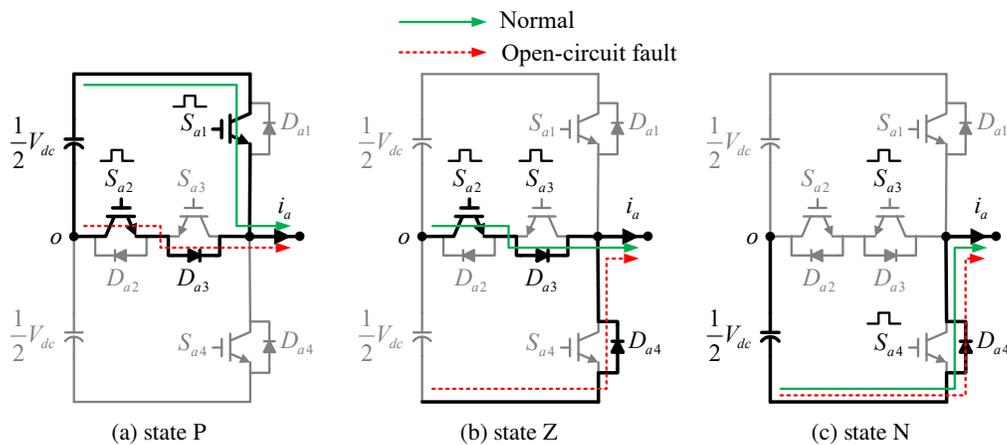


Fig. 2. Current path before and after open-circuit fault of different devices ( $i_a > 0$ ): (a) state P; (b) state Z; (c) state N

When the phase current  $i_a < 0$ , under three different switching states, the change of the phase current path before and after an open-circuit fault, is shown in Fig. 3. In the switching state P, the current flows to the DC power supply through  $D_{a1}$ , so an open-circuit fault that occurs in any device will not affect this state, as shown in Fig. 3(a). In the switching state Z, the phase current flows to the midpoint of the DC power supply through  $S_{a3}$  and  $D_{a2}$  under normal conditions. Only the open-circuit fault of  $S_{a3}$  will affect the state. When an open-circuit fault occurs in  $S_{a3}$ , the phase current freewheels through  $D_{a1}$  as shown in Fig. 3(b). In the switching state N, the phase current flows through  $S_{a4}$  in normal condition. If an open-circuit fault occurs in  $S_{a4}$ , the phase current flows through  $S_{a3}$  and  $D_{a2}$  to the midpoint of the DC power supply as shown in Fig. 3(c).

Combined the above analysis results with the information in Table 1, the impact of the open-circuit fault of different devices in the T-type three-level inverter is shown in Table 2. The column of “faulty device” in Table 2 indicates that the current path and switching state change only when this device fails. For example, the open circuit of  $S_{a1}$  will only affect the phase current  $i_a > 0$  and the switching state is P. The meaning of “any” is that in this case, an open circuit of any device of this phase will not affect the phase current path and switching state.

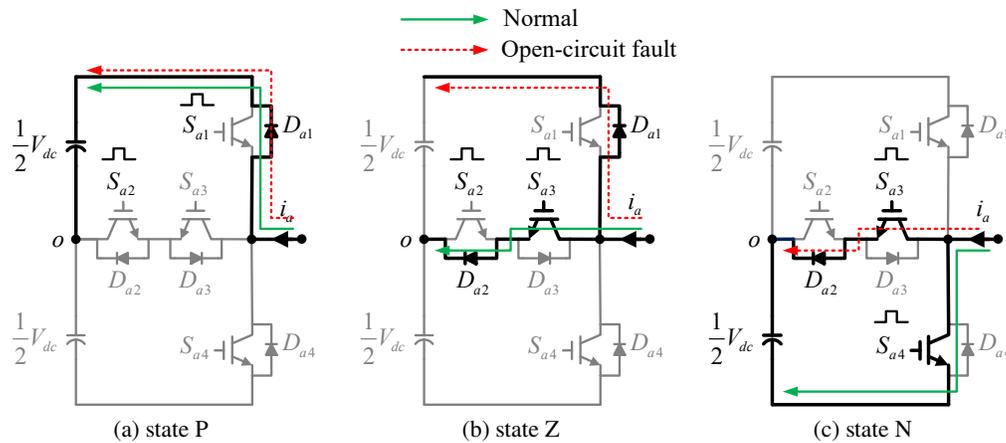


Fig. 3. Current path before and after open-circuit fault of different devices ( $i_a < 0$ ): (a) state P; (b) state Z; (c) state N

Table 2. Influence on the inverter under open-circuit fault of different devices

Phase current direction	Normal			Open-circuit fault			
	Switching state	Current path	Bridge voltage	Faulty device	Current path	Switching state	Bridge voltage
$i_a > 0$	P	$S_{a1}$	$+V_{dc}/2$	$S_{a1}$	$S_{a2}, D_{a3}$	Z	0
	Z	$S_{a2}, D_{a3}$	0	$S_{a2}$	$D_{a4}$	N	$-V_{dc}/2$
	N	$D_{a4}$	$-V_{dc}/2$	any	$D_{a4}$	N	$-V_{dc}/2$
$i_a < 0$	P	$D_{a1}$	$+V_{dc}/2$	any	$D_{a1}$	P	$+V_{dc}/2$
	Z	$S_{a3}, D_{a2}$	0	$S_{a3}$	$D_{a1}$	P	$+V_{dc}/2$
	N	$S_{a4}$	$-V_{dc}/2$	$S_{a4}$	$S_{a3}, D_{a2}$	Z	0

### 3. Fault diagnosis method

According to the results shown in Table 2, the switching state, current path and bridge voltage will be impacted when an open-circuit fault occurs. For example, when the phase current  $i_a > 0$  and  $S_{a1}$  is open-circuited, the switching state changes from P to Z, and the change of the switching state will affect the corresponding bridge voltage. As a result, the bridge voltage will change from  $+V_{dc}/2$  to 0. On the other hand, when the phase current  $i_a < 0$  and  $S_{a3}$  is open-circuited, the switching state changes from Z to P, and the bridge voltage will change from 0 to  $+V_{dc}/2$ . Hence, maybe we can find the faulty device in the inverter according to the bridge voltage.

The above conclusion is obvious and some fault diagnosis methods have been proposed based on the bridge voltage [16–18]. However, the bridge voltage of each phase only represents the fault information of this phase, and the fault diagnosis processing based on bridge voltages must

be carried out phase after phase. Therefore, this paper proposes a unified fault diagnosis method for the open-circuit fault conditions of three-phase devices based on unified consideration of the bridge voltages.

Assuming that the inverter has a common inductive load, the bridge voltage  $v_{ao}$ , the reference voltage  $v_{refa}$  and the phase current  $i_a$  of the a-phase are shown in Fig. 4. Here,  $\varphi$  in the figure is the impedance angle.

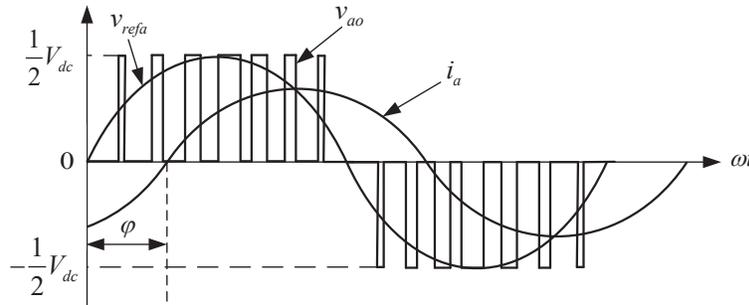


Fig. 4. Waveforms of bridge voltage, reference voltage and phase current of T-type three-level inverter

If bridge voltages are processed in a certain way, considering that there is a fixed phase difference among these voltages, the process result should be able to contain the fault information of these bridge voltages, and the information will also have fixed phase difference. Two calculation results of the bridge voltages are expressed here, as shown in Equation (1) and Equation (2). Both calculation results are used as fault signals for the fault diagnosis of the T-type three-level inverter.

$$v_{\text{sum1}} = |v_{ao}| + |v_{bo}| + |v_{co}|, \quad (1)$$

$$v_{\text{sum2}} = |v_{ao} + v_{bo} + v_{co}|, \quad (2)$$

where  $v_{ao}$ ,  $v_{bo}$ ,  $v_{co}$  are the three bridge voltages.

Based on the PSIM software, both fault signals have been studied whether the T-type three-level inverter is under normal or open-circuit fault conditions. It is found that when the T-type three-level inverter works under normal conditions, the normal value of  $v_{\text{sum1}}$  is between  $0.5 V_{dc}$  and  $1.5 V_{dc}$ , and the normal value of  $v_{\text{sum2}}$  is between  $0$  and  $V_{dc}$ . When  $S_{x1}$  or  $S_{x4}$  ( $x = a, b, c$ ) of the inverter is under open-circuit fault conditions, the value of  $v_{\text{sum1}}$  will be abnormal and between  $0$  and  $0.5 V_{dc}$ . If the open-circuit fault occurs in  $S_{x2}$  or  $S_{x3}$  ( $x = a, b, c$ ), the value of  $v_{\text{sum2}}$  will change between  $V_{dc}$  and  $1.5 V_{dc}$ . In addition, the abnormal value position of  $v_{\text{sum1}}$  and  $v_{\text{sum2}}$  is related to different faulty devices, so the open-circuit fault diagnosis of the inverter can be carried out based on these signals.

Both fault signals shown in Equation (1) and Equation (2) are studied when all devices of the T-type three-level inverter are under open-circuit fault conditions. It is found that when an open-circuit fault occurs in a certain device the inverter works stably, the corresponding value of fault signals and the location of their abnormal value are shown in Table 3. The location of the abnormal value of both fault signals in Table 3 takes the coordinate origin of Fig. 4 as the reference point. In addition, the abnormal value appears in a cycle of  $2\pi$ .

Table 3. Fault information under open-circuit fault

Faulty device	Value of fault signals	Location of abnormal value
$S_{a1}$	$0 < v_{sum1} < 0.5 V_{dc}$	$60^\circ \sim 120^\circ$
$S_{b1}$	$0 < v_{sum1} < 0.5 V_{dc}$	$180^\circ \sim 240^\circ$
$S_{c1}$	$0 < v_{sum1} < 0.5 V_{dc}$	$300^\circ \sim 360^\circ$
$S_{a4}$	$0 < v_{sum1} < 0.5 V_{dc}$	$240^\circ \sim 300^\circ$
$S_{b4}$	$0 < v_{sum1} < 0.5 V_{dc}$	$0^\circ \sim 60^\circ$
$S_{c4}$	$0 < v_{sum1} < 0.5 V_{dc}$	$120^\circ \sim 180^\circ$
$S_{a2}$	$V_{dc} < v_{sum2} < 1.5 V_{dc}$	$60^\circ \sim 120^\circ$
$S_{b2}$	$V_{dc} < v_{sum2} < 1.5 V_{dc}$	$180^\circ \sim 240^\circ$
$S_{c2}$	$V_{dc} < v_{sum2} < 1.5 V_{dc}$	$300^\circ \sim 360^\circ$
$S_{a3}$	$V_{dc} < v_{sum2} < 1.5 V_{dc}$	$240^\circ \sim 300^\circ$
$S_{b3}$	$V_{dc} < v_{sum2} < 1.5 V_{dc}$	$0^\circ \sim 60^\circ$
$S_{c3}$	$V_{dc} < v_{sum2} < 1.5 V_{dc}$	$120^\circ \sim 180^\circ$

Based on Equation (1), Equation (2) and the result shown in Table 3, a fault diagnosis flowchart is proposed, as shown in Fig. 5. Firstly, bridge voltages  $v_{ao}$ ,  $v_{bo}$  and  $v_{co}$  are acquired. Then two fault signals  $v_{sum1}$  and  $v_{sum2}$  are calculated based on Equation (1) and Equation (2). If both fault signals are normal, there is no failure in the inverter. And if any fault signal is abnormal, it can be concluded which device has an open-circuit fault based on the information shown in Table 3.

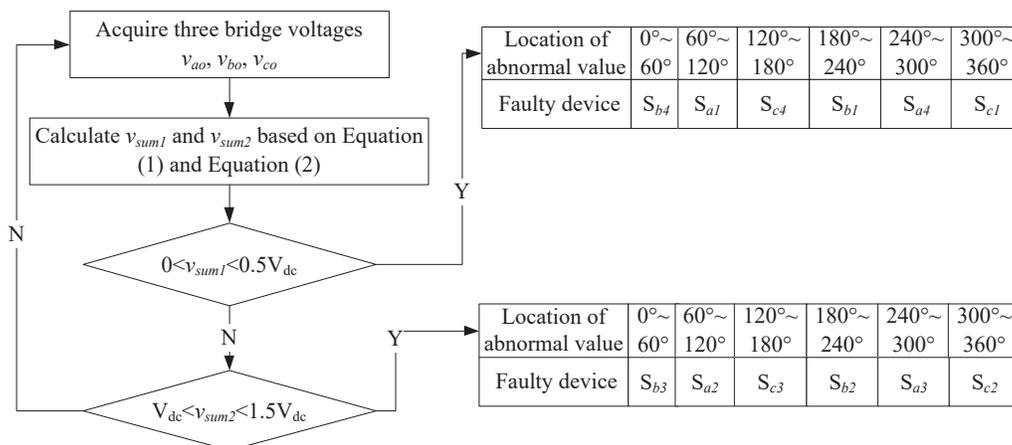


Fig. 5. Fault diagnosis flowchart

#### 4. Simulation results

A T-type three-level inverter is set up using the PSIM software, with the input DC voltage  $V_{dc}$  100 V, each phase load  $8 \Omega$  resistor in series with 20 mH inductance. The output voltage fundamental frequency is 50 Hz and the carrier frequency is 6 kHz. Fig. 6 shows the waveforms of three bridge voltages and two fault signals under normal operating conditions. It can be seen that under normal conditions, the bridge voltages are normal three-level waveforms, the value of  $v_{sum1}$  is between 50 V and 150 V and the value of  $v_{sum2}$  is between 0 and 100 V.

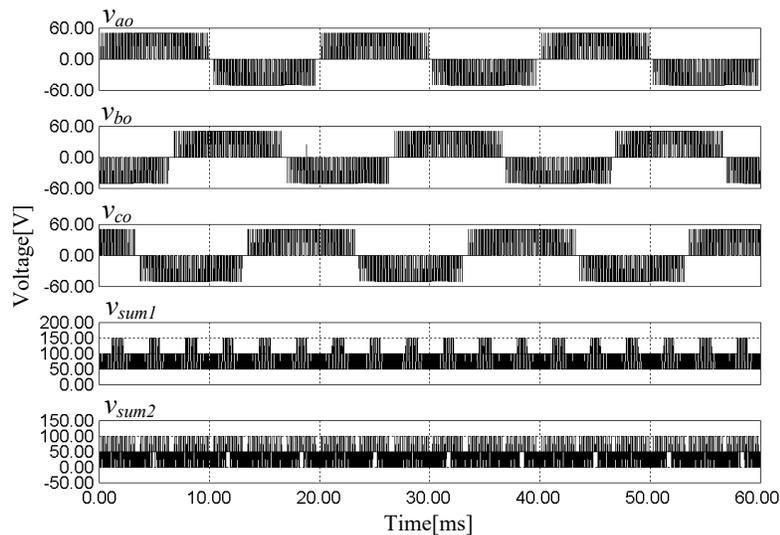


Fig. 6. Simulation results when the inverter works normally

Fig. 7 and Fig. 8 show the waveforms of the simulation results when the devices  $S_{a1}$  and  $S_{a4}$  are under open-circuit fault conditions, respectively. The fault occurrence time of the open-circuit, named as  $T_{Fault}$ , is 20 ms, as shown in Fig. 7 and Fig. 8. It can be seen that when an open-circuit fault occurs in the above devices, the bridge voltages of the corresponding phase is distorted and the fault signal  $v_{sum1}$  has an abnormal value between 0 and 50 V. Obviously, location of this abnormal value is related to the different device.

In Fig. 7, the device  $S_{a1}$  is under open-circuit fault conditions and it can be known from Table 2 that the switching state will change from P to Z and the bridge voltage  $v_{ao}$  will change from  $+V_{dc}/2$  to 0 when the phase current is positive. As a result, there is a relatively long time zero level in the bridge  $v_{ao}$ . Similarly, in Fig. 8, the device  $S_{a4}$  is under open-circuit fault conditions and it can be known from Table 2 that the bridge voltage  $v_{ao}$  will change from  $-V_{dc}/2$  to 0 when the phase current is negative. As a result, there is a relatively long time zero level in the bridge  $v_{ao}$  too.

Another different load is considered here (inductance of the load is changed to 10 mH). Fig. 9 shows simulation waveforms when  $S_{a1}$  is under open-circuit fault conditions. Compared to Fig. 7, it can be seen that the bridge voltage  $v_{ao}$  is a little different but the fault signal  $v_{sum1}$  is the same.

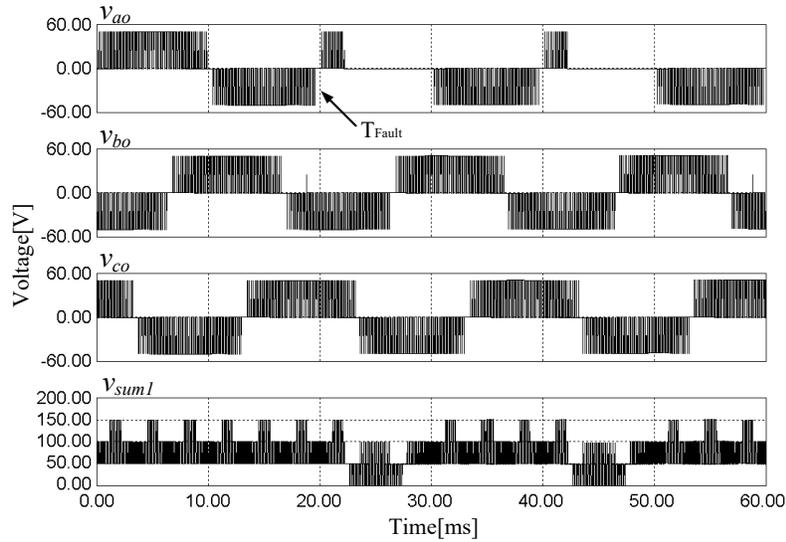


Fig. 7. Simulation results when  $S_{a1}$  is open-circuited

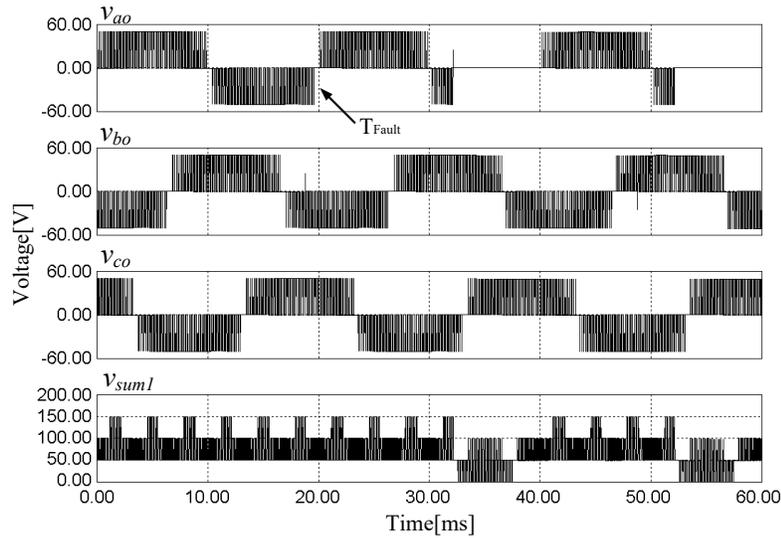


Fig. 8. Simulation results when  $S_{a4}$  is open-circuited

The fault signals  $v_{sum1}$  are combined using Matlab and the result is shown in Fig. 10. In this figure, the waveforms from top to bottom are fault signals when  $S_{a1}$ ,  $S_{b1}$ ,  $S_{c1}$ ,  $S_{a4}$ ,  $S_{b4}$  and  $S_{c4}$  are under open-circuit fault conditions, respectively. The time coordinate of Fig. 10 is the same as Fig. 7 and Fig. 8, so we take the fault occurrence time 20 ms as the reference point ( $0^\circ$ ). It can be seen from Fig. 10 that when the corresponding device is under open-circuit fault conditions,

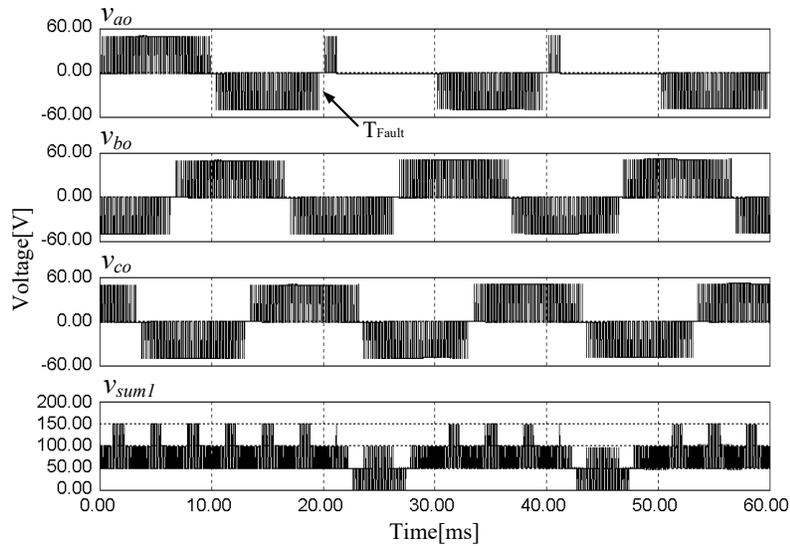


Fig. 9. Simulation results when  $S_{a1}$  is open-circuited with a different load

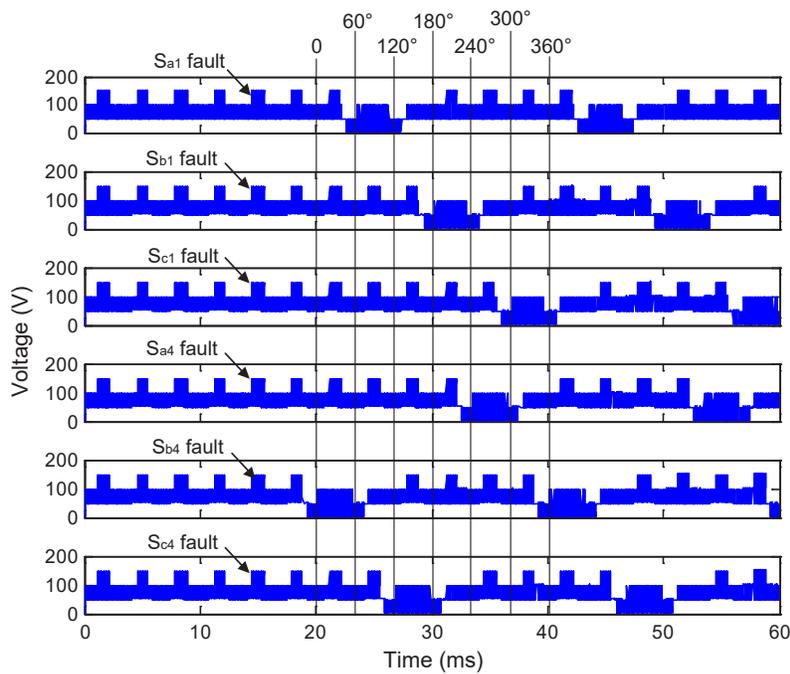


Fig. 10. Comparison of the fault characteristic signal  $v_{sum1}$  when an open-circuit fault occurs on different devices

the location of the abnormal value of  $v_{sum1}$  is the same as shown in Table 3. For example, when the device  $S_{a1}$  is under open-circuit fault conditions, the location of the abnormal value in  $v_{sum1}$  is from  $60^\circ$  to  $120^\circ$ , just as “ $60^\circ \sim 120^\circ$ ” shown in Table 3. In fact, only the middle part of the abnormal value in  $v_{sum1}$  falls within the location given in Table 3, and both sides are slightly exceeded. However, it does not affect the result of the fault diagnosis.

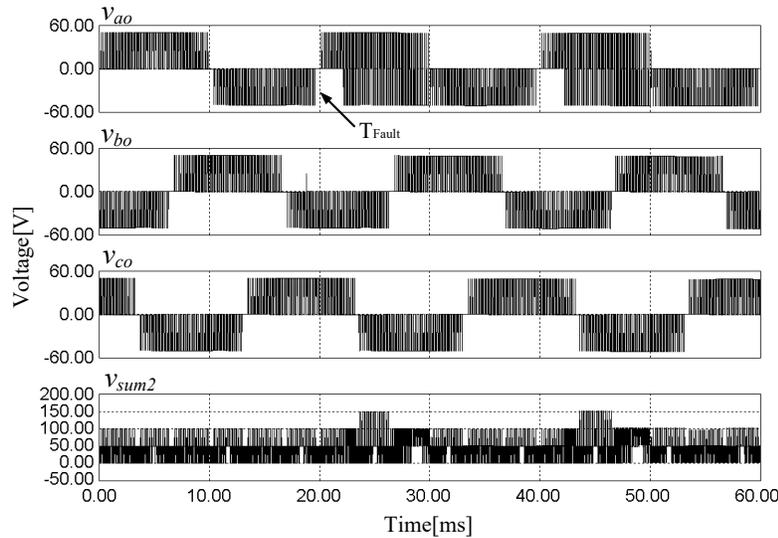


Fig. 11. Simulation results when  $S_{a2}$  is open-circuited

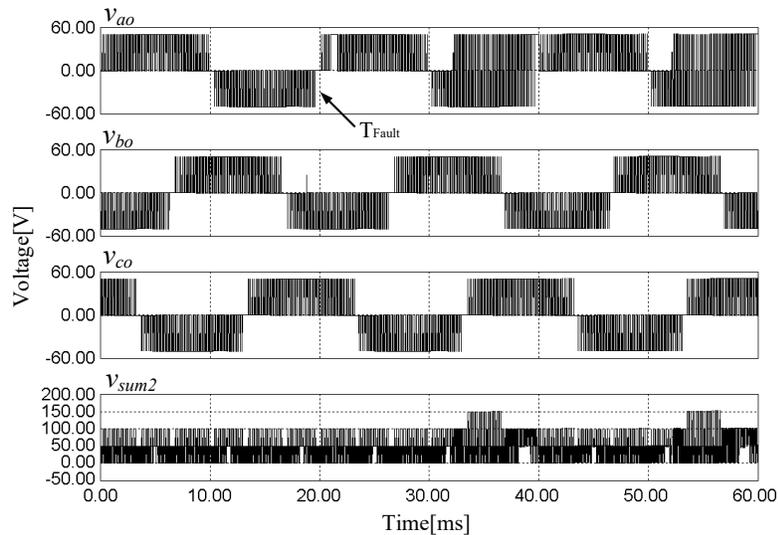


Fig. 12. Simulation results when  $S_{a3}$  is open-circuited

Fig. 11 and Fig. 12 show the waveforms of the simulation results when the devices  $S_{a2}$  and  $S_{a3}$  are under open-circuit fault conditions, respectively. The fault occurrence time of the open-circuit  $T_{\text{Fault}}$  is 20 ms as shown in Fig. 11 and Fig. 12. It can be seen that when the open-circuit fault conditions occur in these devices, the bridge voltages of the corresponding phase are distorted and the fault signal  $v_{\text{sum}2}$  has an abnormal value between 100 V and 150 V and the location of this abnormal value is related to the different device too.

In Fig. 11, the device  $S_{a2}$  is under open-circuit fault conditions and it can be known from Table 2 that the switching state will change from Z to N and the bridge voltage  $v_{ao}$  will change from 0 to  $-V_{\text{dc}}/2$  when the phase current is positive. As a result, there is a relatively long time when the bridge  $v_{ao}$  is alternating between  $+V_{\text{dc}}/2$  and  $-V_{\text{dc}}/2$ . Similarly, in Fig. 12, the device  $S_{a3}$  is under open-circuit fault conditions and it can be known from Table 2 that the bridge voltage  $v_{ao}$  will change from 0 to  $+V_{\text{dc}}/2$  when the phase current is negative. As a result, there is a relatively long time when the bridge  $v_{ao}$  is alternating between  $+V_{\text{dc}}/2$  and  $-V_{\text{dc}}/2$  too.

The different load with the inductance is 10 mH is also considered when  $S_{a2}$  is under open-circuit fault conditions, the simulation waveforms are shown in Fig. 13. Compared to Fig. 11, it can be seen that the bridge voltage  $v_{ao}$  is a little different but the fault signal  $v_{\text{sum}2}$  is the same.

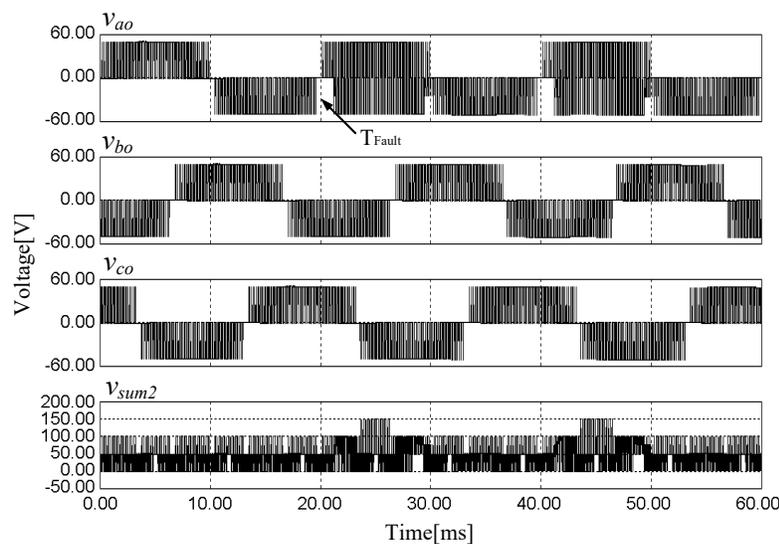


Fig. 13. Simulation results when  $S_{a2}$  is open-circuited with a different load

The fault signals  $v_{\text{sum}2}$  are combined using Matlab and the result is shown in Fig. 14. In this figure, the waveforms from top to bottom are fault signals when  $S_{a2}$ ,  $S_{b2}$ ,  $S_{c2}$ ,  $S_{a3}$ ,  $S_{b3}$  and  $S_{c3}$  are under open-circuit fault conditions, respectively. It can also be seen from Fig. 14 that when the corresponding device is under open-circuit fault conditions, the location of the abnormal value of  $v_{\text{sum}2}$  is the same as shown in Table 3. For example, when the device  $S_{a2}$  is under open-circuit fault conditions, the location of the abnormal value in  $v_{\text{sum}2}$  is from  $60^\circ$  to  $120^\circ$ .

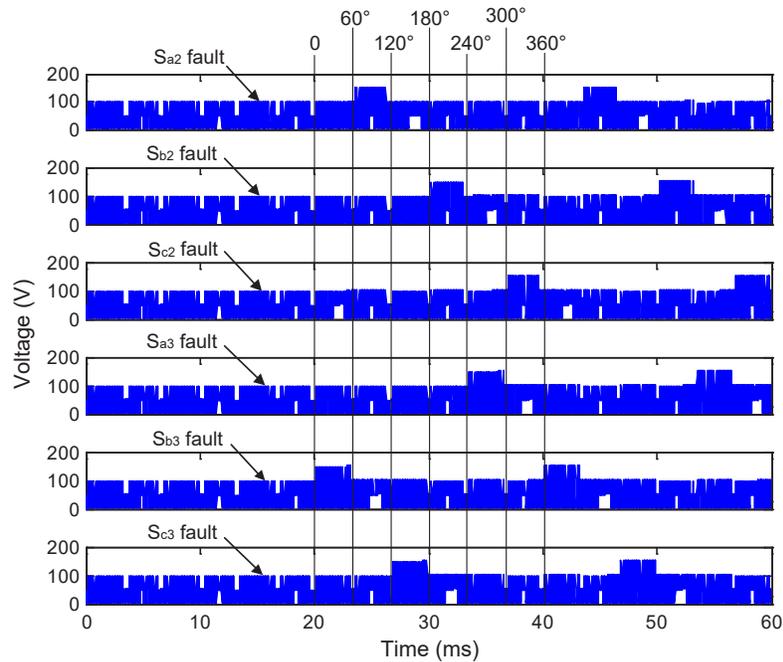


Fig. 14. Comparison of the fault characteristic signal  $v_{sum2}$  when an open-circuit fault occurs on different devices

## 5. Conclusions

Two different fault signals are obtained based on the bridge voltages of a T-type three-level inverter. Using these two kinds of fault signals, this paper proposes an open-circuit fault diagnosis method for the T-type three-level inverter. In the diagnosis processing one phase follows another if only using the bridge voltage independently. In addition, the fault characteristics of the bridge voltage are relatively difficult to distinguish from the normal condition. Based on the two kinds of fault signals proposed in this paper, the open-circuit fault of the inverter devices can be diagnosed in a unified way. The fault characteristics of the two kinds of fault signals are easy to distinguish from the normal conditions. As long as a reasonable threshold is set and the location of the abnormal value of fault signals are detected, the specific device under open-circuit fault conditions can be located.

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**References**

- [1] Karthik A., Loganathan U., *A reduced component count five-level inverter topology for high reliability electric drives*, IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 725–732 (2020).
- [2] Jin H., Luo Y., Yan Y., Pan S., *Improved carrier phase shift modulation and voltage equalization control strategy in modular multilevel converter*, Archives of electrical engineering, vol. 68, no. 4, pp. 803–815 (2019).
- [3] Majumder M.G., Yadav A.K., Gopakumar K., Raj R.K., Loganathan U., Franquelo L.G., *A 5-level inverter scheme using single DC link with reduced number of floating capacitors and switches for open-end IM drives*, IEEE Transactions on Industrial Electronics, vol. 67, no. 2, pp. 960–968 (2020).
- [4] Lewicki A., Morawiec M., *Structure and the space vector modulation for a medium-voltage power-electronic-transformer based on two seven-level cascade H-bridge inverters*, IET Electric Power Applications, vol. 13, no. 10, pp. 1514–1523 (2019).
- [5] Li X., Xing X., Zhang C., Chen A., Qin C., Zhang G., *Simultaneous common-mode resonance circulating current and leakage current suppression for transformerless three-level T-type PV inverter system*, IEEE Transactions on Industrial Electronics, vol. 66, no. 6, pp. 4457–4467 (2019).
- [6] Qin S., Lei Y., Ye Z., Chou D., Pilawa-Podgurski R.C.N., *A high-power-density power factor correction front end based on seven-level flying capacitor multilevel converter*, IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1883–1898 (2019).
- [7] Kim H., Kwon Y., Chee S., Sul S., *Analysis and compensation of inverter nonlinearity for three-level T-type inverters*, IEEE Transactions on Power Electronics, vol. 32, no. 6, pp. 4970–4980 (2017).
- [8] Wang B., Li Z., Bai Z., Krein P.T., Ma H., *A redundant unit to form T-type three-level inverters tolerant of IGBT open-circuit faults in multiple legs*, IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 924–939 (2020).
- [9] Wang B., Li Z., Bai Z., Krein P.T., Ma H., *Real-time diagnosis of multiple transistor open-circuit faults in a T-type inverter based on finite-state machine model*, CPSS Transactions on Power Electronics and Applications, vol. 5, no. 1, pp. 74–85 (2020).
- [10] Choi U., Lee K., Blaabjerg F., *Diagnosis and tolerant strategy of an open-switch fault for T-type three-level inverter systems*, IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 495–508 (2014).
- [11] He J., Demerdash N.A.O., Weise N., Katebi R., *A fast on-line diagnostic method for open-circuit switch faults in SiC-MOSFET-based T-type multilevel inverters*, IEEE Transactions on Industry Applications, vol. 53, no. 3, pp. 2948–2958 (2017).
- [12] Wang K., Tang Y., Zhang C., *Open-circuit fault diagnosis and tolerance strategy applied to four-wire T-type converter systems*, IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5764–5778 (2019).
- [13] Wang X., Wang Z., Xu Z., He J., Zhao W., *Diagnosis and tolerance of common electrical faults in T-type three-level inverters fed dual three-phase PMSM drives*, IEEE Transactions on Power Electronics, vol. 35, no. 2, pp. 1753–1769 (2020).
- [14] Schweizer M., Kolar J.W., *Design and implementation of a highly efficient three-level T-type converter for low-voltage applications*, IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 899–907 (2013).

- 
- [15] Wang K., Tang Y., Zhang C., *Open-circuit fault diagnosis and tolerance strategy applied to four-wire T-type converter systems*, IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5764–5778 (2019).
- [16] Abadi M.B., Mendes A.M.S., Cruz S.M.Â., *Method to diagnose open-circuit faults in active power switches and clamp-diodes of three-level neutral-point clamped inverters*, IET Electric Power Applications, vol. 10, no. 7, pp. 623–632 (2016).
- [17] Zhou D., Yang S., Tang Y., *A voltage-based open-circuit fault detection and isolation approach for modular multilevel converters with model-predictive control*, IEEE Transactions on Power Electronics, vol. 33, no. 11, pp. 9866–9874 (2018).
- [18] Chen D., Liu Y., Zhang S., *Open-circuit fault diagnosis method for the T-type inverter based on analysis of the switched bridge voltage*, IET Power Electronics, vol. 12, no. 2, pp. 295–302 (2019).