

Opto-Electronics Review

journal homepage: https://journals.pan.pl/opelre



Analysis of reducing common mode noise of conducted emission in a switching power converter considering parasitic effects

G. V. Aswini^{*}, S. Chenthurpandian

Department of Electronics and Communication Engineering, SNS College of Technology, Coimbatore-641035, India

Article info	Abstract
Article history: Received 24 Apr. 2023 Received in revised form 04 Aug. 2023 Accepted 07 Aug. 2023 Available or Jine 21 Sep. 2022	Most automotive electronic components can cause electromagnetic interference, that cause power electronic circuits to become unstable. As per electromagnetic compatible (EMC) standards, these electronic circuits should meet the specifications which are achieved under some conditions. In this paper, the conducted emissions (CEs) are generated as the specification of the specification o
Keywords: Conducted emission; radiated emission; electromagnetic interference; electromagnetic compatibility; EMI filter.	due to the switching of a buck converter, which often occurs in automotive electronics. The noise source was found to be due to the presence of common mode currents which largely affects the performance of EMC. Two types of filtering techniques were analysed and designed, and the results were compared to find an effective filtering solution to mitigate the effects of CE due to a common mode noise for the frequency range from 150 kHz to 108 MHz according to the International Special Committee on Radio Interference (CISPR25) standard. The capacitive and parasitic impedance were calculated and then used in the simulation. Finally, the simulated and measured results are presented. The noise level can be minimized by as much as 50 dB, which is an efficient noise reduction value.

1. Introduction

In fields such as telecommunications [1] automotive [2, 3], and aeronautics [4] high power density and high efficiency are critical requirements in power converters. To reduce passive space and weight without increasing converter switching losses, current efforts are aimed at using higher switching frequencies and quick switches [5]. Alternatively, high switching frequencies can cause conducted and radiated emissions due to rapid changes in voltage and current [6].

In addition to this, silicon carbide [7], which is the emerging power electronic component, has also created severe electromagnetic compatibility (EMC) problems. Due to these components, the conducted emission (CE) due to common mode (CM) noise and differential mode (DM) noise is increased to a greater extent. This occurs mainly because of the high speed switching and new operating point at high frequencies of silicon carbide. Moreover, the power electronic components also generate the differential DM and CM currents which circulate via ground loops and generate serious electromagnetic interference (EMI) problems [8].

Variations in dv/dt which interact with parasitic elements of the routing, strongly influence the CM currents generated at power semiconductor components. Capacitive CM coupling allows higher frequency ranges than DM current for parasitic capacitances which vary significantly with frequency. As a result, CM currents are responsible for a significant amount of electromagnetic radiation. Hence, the CM current influence must be minimized.

In general, strategies aiming at reducing CEs of converters are evaluated [9-12] at the converter input leads for different modes [13-15].

Yazdani *et al.* [16] proposed development of filtering approaches to mitigate the effects of reduced equivalent noise sources at converter input power leads. In a forward converter, the voltage difference between the output terminals is reduced due to inductor symmetrisation, although the underlying mechanism of this phenomenon

^{*}Corresponding author at: gvaswini37@gmail.com

https://doi.org/10.24425/opelre.2023.147039

^{1896-3757/} Association of Polish Electrical Engineers (SEP) and Polish Academic of Sciences (PAS). Published by PAS

^{© 2023} The Author(s). This is an open access article under the CC BY license (https://creativecommons.org/licenses/by/4.0/).

is not completely investigated. There have been several approaches to EMI mitigation for power converters, including transformerless active EMI filter (AEF) which is based on the virtual impedance enhancement concept [17], printed circuit board (PCB)-based planar CM EMI filtering for SiC inverters/rectifiers [18], pseudo-random modulation and soft switching for buck converters [19], and an improved radiated EMI model with the PCB ground impedance active-clamp flyback (ACF) power converters [20]. From this, electromagnetic radiation is mainly caused by CM currents. It is necessary to solve the problem of CM currents circulating in a cable. This paper presents a novel topology to reduce the effect of EMI in power converters, a common automotive electronic component.

The high switching speed buck converter conducted and radiated EMI emissions caused by the CM current are expected to achieve this goal. Therefore, parasitic effects of different components are calculated. To reduce the EMI effect, two types of filtering topologies such as an input EMI filter and RF inductors are used. The performance of these filters is verified using simulation. Simulation program with integrated circuit emphasis (SPICE) is used to simulate both active and passive components in the time domain.

The main contribution of the proposed work is described below:

- To solve the EMI emissions problem caused by the CM current in high switching speed buck converter fed, an automotive application technique is proposed.
- To decrease the EMI effect, a filtering topology, such as an input EMI filter and RF inductors, is proposed.
- The parasitic effects of different elements are calculated and the same were used in the simulation.
- The performance of these filters is verified using simulation. SPICE is used to simulate both active and passive components in the time domain.
- Identification of EMC design, prediction of EMI created by power electronic circuit (PEC), and the optimization criteria for power converters based on their intended usage are presented.

The rest of the paper is organised as below. Section 2 describes the CE of the buck converter. Section 3 provides the proposed circuit modelling techniques. Section 4 describes the measurement and setup validation for the proposed model. Section 5 defines the mitigation methods of CM EMI effects. Section 6 discusses the simulation results of the proposed method. Finally, section 7 provides the conclusion and future work.

2. CE in buck converters.

Conducted EMI is injected by the switching circuit of the buck converter, which propagates through conductors inside the entire network mainly through power lines. Though the switching speed is less than 1 MHz in a modern buck converter design, the rise and fall time vary from micro- to nano-second range which introduces EMI from a few kHz to hundreds of MHz. This study deals with the mitigation of EMI in buck converters by considering the same configuration used in an electric vehicle (EV) and hybrid vehicles. In addition to the lumped elements, parasitic capacitance and inductance effects on PCB are also considered. The automotive buck converters adhere to the standard CISPR25 [21–23].

Usually, an expensive suppression filter is used to reduce the disturbance in the input side and there is no guarantee of EMI compliance. Hence, the noise in the input stage as line impedance stabilization network (LISN) is analysed and a model is developed to reduce it.

Figure 1 shows the buck converter design considering capacitive and inductive parasitic impedance including the proposed model of LISN, cable, parasitic capacitance, parasitic impedance, and semiconductor component (P-channel MOSFET). In the below figure, the parasitic impedances ZpL1 to ZpL5 are represented for routing [24, 25]. In the Simscape library of MATLAB Simulink, the SPICE models of power electronic switches are not compliant to this simulation since they do not take EMC effects into account.



Fig. 1. Buck converter design considering capacitive and inductive parasitic impedance.

The voltage signal of value Vdc is modulated by the voltage at the gate terminal of MOSFET, Vpulse. Vpulse is the square wave with period T and duty cycle τ/T which is equal to a switching frequency of 100 kHz and 30% duty cycle. When MOSFET is ON (Vpulse value at peak), the diode D1 is reverse biased. When the MOSFET is OFF, the diode is forward biased. Hence, by adjusting the duty cycle of MOSFET, the average value of Vdc can be controlled. Thus, the switching frequency and duty cycle play a vital role here. This also comprises the noise induced into the circuit.

CE from the switching buck converter may be narrowband and broadband. Emission in the broadband is mainly due to the diode and other parasitic phenomena which is hard to analyse theoretically. This type of emissions can be minimized by adhering to proper design rules such as good layout, shielding, and grounding. By doing so, the product does not surpass the standard limit as per CISPR25. In this study, the effect of narrowband emission which is due to the switching of the buck converter is analysed. Unlike broadband, narrowband emission is large which may cause the product to fail during the EMC test.

3. Circuit modelling

3.1. Calculation of parasitic effects

3.1.1. Effects of parasitic capacitance

The effects of parasitic capacitance depend on the layout of the power converter [26]. Since the geometrical structure of the converter is simple, analytical methods were used to calculate the parasitic capacitance [27, 28] and edge effects were also included in some formulas [29].

The rise and fall timings of the signal are empirically calculated in this model, and the driver employs a trapezoidal signal. These timings have a direct impact on EMI effects because they alter the switching rates of semiconductor components. Beyond 3 MHz, the extracted waveform spectrum changes by $12\;dB\mu V$ between measurement and simulation. Compared to the basic circuit, the proposed circuit layout replaces the control switch JFET [30] with a MOSFET to improve performance. According to Fig. 2, four capacitances are present between track and ground, and four capacitors are present between tracks. For calculating the capacitance between the track and reference ground, a model is shown in Ref. 27. The capacitance (C) value is calculated using (1) and this value has been validated through the measurement which shows the best results due to edge-effect consideration.

$$C = \varepsilon_0 \varepsilon_r \left[1.15 \frac{W}{h} + 2.8 \left(\frac{t}{h}\right)^{0.222} \right] L, \tag{1}$$



Fig. 2. Circuit layout: (a) parasitic capacitance between tracks and reference ground, (b) parasitic capacitance between tracks.

where $\varepsilon_0\varepsilon_r$ is the dielectric constant ($\varepsilon_0 = 8.85419 \cdot 10^{-12}$ F/m and $\varepsilon_r = 4.7$) [17, 18, 28], W is the width of the track, L is the length of the track, h is the height between the track and ground, and t is the thickness of the track.

To find the equivalent capacitance between track and ground, i.e., C_{01} , the following (2) can be used:

$$C_{01} = \varepsilon_0 \varepsilon_r \left[1.15 \frac{W}{h} + 2.8 \left(\frac{t}{h} \right)^{0.222} \right] L + \left[1.15 \frac{W'}{h} + 2.8 \left(\frac{t}{h} \right)^{0.222} \right] L',$$

$$(2)$$

where *W*' and *L*' are the width and length of the ground plane. The dimensions used in (2) are W = 37.5 mm, L = 75.5 mm, W' = 22.5 mm, L' = 8 mm, and h = 1.57 mm. By applying the above dimensions to (2), one gets $C_{01} = 95.56$ pF. In this same way, other capacitances such as C_{02} , C_{03} , and C_{04} are calculated.

Similarly, the coupling capacitance between tracks can be calculated using the equation used in Ref. 8 which gives

$$C_{mn} = \varepsilon_0 \varepsilon_r \left(1.17 \left(\frac{W}{h} \right)^{0.0836} \cdot \left[\frac{S}{h} + 0.402 \right]^{-0.78} + \left(\frac{S}{h} + 1.32 \right)^{-0.8} \cdot \left[-1.36 \left(\frac{W}{h} \right)^{-0.037} + 0.227 \left(\frac{t}{h} \right)^{0.98} \right] \right).$$
(3)

Here *S* is the spacing between tracks.

3.1.2. Effects of parasitic inductance

By the values calculated from the formula using the low frequency method [31, 32], the inductive (self and mutual inductance) model can be simulated. A resistive model can also be determined from Ref. 32. RL network can be used to determine the parameters which occur because of skin effect [33]. The value of parasitic inductance calculated for the circuit in Fig. 2 is given below [34]:

$$\frac{L_{\text{para}}}{\mu_0} = 3.71 \left(\frac{h}{W}\right)^{0.041} + 0.018 \left(\frac{h}{W}\right)^{-0.73} - 3.39 \left(\frac{h}{t}\right)^{-0.0006} + \exp\left(-1.89\frac{S}{h}\right) \cdot \left[0.75 \left(\frac{h}{W}\right)^{-0.00052} - 0.84 \left(\frac{h}{t}\right)^{-0.026}\right].$$
(4)

$$\frac{L_{\text{mutual}}}{\mu_{0}} = \left[-0.415 \left(\frac{h}{W}\right)^{-0.16} - 2.38 \left(\frac{t}{W}\right)^{1.18} \cdot \left(\frac{S}{h} + 1.07\right)^{-2.6} + \left(\frac{S}{h} + 0.89\right)^{-2.03} \cdot \left[0.418 \left(\frac{h}{W}\right)^{0.13} + 1.37 \left(\frac{t}{W}\right)^{1.09} \right] \right]$$
(5)

The value of parasitic mutual inductance is calculated for the circuit in Fig. 1 given above.

The track parasitic resistance is given by the formula:

$$R_{\text{para}} = \sqrt{\rho \cdot \mu_0} \cdot \pi \cdot f\left(\frac{L}{W}\right). \tag{6}$$

The skin depth is considered in the above equation which is dependent on frequency.

3.1.3. Modelling of unshielded energy cables

The model of the unshielded cable in low frequency (600 kHz) is used as shown in Ref. 35. The RL ladder network modelled considering the skin and proximity effects of a basic cell is shown in Fig. 3. Analytical calculations are used to compute the electrical parameters per unit length in low frequency (600 kHz) cable modelling. In this work, 200 mm cable (for the voltage method) and 2000 mm cable (for the current probe method) are considered and simulated using 32 cells.



Fig 3. RL ladder network used to model skin and proximity effect of the basic cell.

4. Measurement setup and validation

The experimental setup of conducting the CE test (Current probe method) as per CISPR25 standard is shown in Fig. 4. It consists of a device under test DUT (DC-DC converter) which is placed on low permittivity support ($\varepsilon_r \le 1.4$) situated 50 mm above the ground plane. The wiring harness which connects LISN and DUT is 200 mm long, it is also placed above low permittivity support ($\varepsilon_r \le 1.4$) situated 50 mm above the ground plane. As per the CISPR25 standard, the CE test is of two types. They are the current probe and voltage method.



Fig. 4. CE measurement setup as per CISPR25 (current probe).

To start with the experiment, the current probe is fixed on the complete wiring harness at a distance of 50 mm near the DUT.

The purpose of using the current probe first is discussed in section 5. Thus, the input EMI filter is calculated by using the cut-off frequency (measured using the current probe method).

The next step is to measure the noise voltage using the voltage method. The experimental setup of CE using the voltage method is shown in Fig. 5. The only difference in the voltage method is that the noise voltage is measured





Fig. 5. (a) CE measurement setup (voltage method); (b) DUT

across 25 Ω of the LISN (for CM noise). The resulting frequency spectrum is measured using a spectrum analyser which displays the noise voltage in dB μ V.

LISN is connected to the 48 V DC battery and the DUT (DC-DC Converter). The DUT is connected to the load box which replicates real-time scenarios. The EMI receiver is connected to the LISN which is used to measure the noise voltage.

5. Methods to mitigate CM EMI effects.

In this section, two approaches are used to mitigate CM EMI effects. The first approach is using EMI filters [16] to mitigate the noise generated by the power converters such as CM noise. For the filter design, the first step is to distinguish the modes of CE. As shown in Fig. 6, CM current (I_{CM}) is measured using a current probe at the positive and negative terminals of LISN. To focus on CM, the proposed filter is designed that considers the CM noise. In this work, one coupled CM inductor (L_{CM}) and two Cy capacitors are connected to the ground. In the CM case, the Cy capacitor is used to reduce the leakage current to the ground. Once the filter values are calculated, they are simulated using SPICE, and the fast Fourier transform (FFT) of the output is obtained. According to EMC



Fig. 6. Current probe used for CM and DM measurement.

standards, the measurement is done using LISN. A spectrum analyser is used to measure CM noise in a frequency band from 150 kHz to 108 MHz as per CISPR25.

The second approach uses an RF inductor which is connected to the ground so that the effect of CM noise is reduced. The purpose of using an RF inductor is that it stops the $I_{\rm CM}$ from returning through the ground loops. By doing so, the magnetic fields radiated by those ground loops are reduced. Filter characteristics are shown in Fig. 7.



Fig. 7. Filter characteristics.

5.1. Calculation of parasitic effects

Figure 8 shows the equivalent circuit of LISN and CM filter. The voltage at the resistor of LISN is calculated from the current probe measurement for CM noise. This measurement is done without the EMI filter. The voltage is calculated from a current probe by using the expression $V_{\text{CM}} = 25\Omega \cdot I_{\text{CM}}$.



Fig. 8. Equivalent circuit of LISN and CM filter.

In this case, the *Cy* value is selected to be 47 μ F for limiting the leakage current to the ground. Hence, from the value *Cy* and cut-off frequency (obtained from the plot), the value of *L*_{CM} can be calculated using the equation

$$L_{\rm CM} = \left(\frac{1}{2\pi f_{\rm CM}}\right)^2 \cdot \frac{1}{2Cy}.$$
 (7)

The summarised values of CM filters such as L_{CM} is 0.1 nH, and Cy is 47 μ F.

By minimizing parasitic inductances and capacitance, an optimal layout design reduces EMI interference.

5.2. *RF inductor*

A small RF inductor is connected between the converter chassis ground and the Earth's reference ground as shown in Fig. 9. By doing so, the conducted EMI effects due to switching noise get reduced.



Fig. 9. Schematic representation showing RF inductor used to reduce CM noise.

The inductor used in this work is VLS5045EX-221M-H whose equivalent circuit and its characteristic values are shown in Fig. 10. In the circuit, an unshielded cable is used so that CM currents return by ground reference plane only. Therefore, all CM current loops can be filtered.



Fig. 10. (a) Equivalent circuit of the inductor, and (b) characteristic values of inductor used in this model.

6. Comparison of simulated and measured results

A comparison of measured and simulated CE data without EMI filter, with EMI filter, and with RF inductor shows promising results as the difference between the results is less than 15 dBµV, mainly in the lower frequency range. The lower frequency mainly relates to the noise voltage exceeding the CISPR25 limit, particularly in the range from 150 kHz to 2 MHz. After 2 MHz, the noise voltage is very low when compared to CISPR25 limits. Figure 11 shows the CE exceeding the limit of EMC standard mainly in the low frequency range, i.e., 150 kHz to 1 MHz which is indicated by the red line. From Fig. 11, if a line at 40 dB/dec is tangent to the curve and when it cuts the frequency axis, that point gives the cut-off frequency. From Fig. 11, the cut-off frequency that was calculated was $f_{CM} = 1.5$ MHz. Hence, the value of $L_{\rm CM} = 0.1$ nH was deduced. The spectrum shown in Fig. 12 signifies the CE noise measured using an EMI receiver at LISN with an EMI filter used in DUT. Similarly, Figure 13



Fig. 11. CM noise at LISN terminal without filter.



Fig. 12. Measured and simulated CM noise at LISN with EMI filter.



Fig. 13. Measured and simulated CM noise at LISN with RF inductor.

signifies the CE noise measured using an EMI receiver at LISN with an RF inductor used in DUT.

From Figs. 9, 12, and 13, it is evident that the efficiency of the RF inductor is very good as the level of the noise made by the DC-DC converter to the battery is lower than the CISPR25 limit. Also, to know the attenuation of the CM filter, the current (I_{CM}) was calculated. From the current, the CM voltage (V_{CM}) ($V_{CM} = 25\Omega I_{CM}$) can be calculated which is shown in Fig. 11. From Figs. 12 and 13, the CE noise is more in the frequency range from 0.15 MHz to 2 MHz. After 2 MHz frequency, the noise voltage gradually reduces and goes down. The goal of this work is to reduce the noise in the low frequency range. Hence, the EMI filter is designed to stop the noise at that particular frequency. This is achieved and the results can be seen in Figs. 12 and 13.

Table 1 shows the comparison of CM noise measured with EMI filter and RF inductor. From Table 1, the frequency range of 0.2 and 0.53 MHz is seriously taken into account because the limit set by CISPR25 has been exceeded in this frequency range.

 Table 1.

 Comparison of the common mode noise without filter, with EMI filter and RF inductor

	Frequency (MHz)			
	0.2	0.53	5.9	76
Noise voltage measured without filter $(dB\mu V)$	74	58	18	-12
Noise voltage measured with EMI filter ($dB\mu V$)	31	18	-29	-54
Improved effect using EMI filter (dBµV)	43	40	47	42
Noise voltage measured with RF inductor $(dB\mu V)$		10	-36	-62
Improved effect using RF inductor (dBµV)	50	48	54	50

Due to the RF inductors, the ground loops are unable to return CM currents, so they radiate fewer magnetic fields. However, the noise voltage from 5.9 and 76 MHz lies below the limits of CISPR25. Comparing the CM noise voltage measured with and without filter shows an improved effect of 43 dB μ V in 0.2 MHz frequency and 40 dB μ V in 0.53 MHz frequency. This gives a promising result when compared with Refs. 1 and 2, as they show only 32 dB μ V and 35 dB μ V improvement after using a filter.

7. Conclusions

In this paper, a designed model of CM noise suppression EMI filter and RF inductor is presented. The entire model of CE from the DC-DC buck converter has been simulated using SPICE software. The SPICE model of LISN is modelled and connected between the power supply and DUT. The simulation was done using the input EMI filter and RF inductors methods and the results were analysed. Finally, the measurement of CM noise was carried out in the anechoic chamber as per CISPR25. Moreover, the DC-DC converter did not produce as much noise as the CISPR25 limits due to the high efficiency of the RF inductor. The model validation was done by comparing the simulation results of CM noise voltage with that measured ones. This validation gives proof that the simulation model used is accurate to find the CM noise spectrum. From the simulation results, the EMI filter is designed to stop the noise at that particular frequency. Hence, these simulation models can be used at the development stage to predict the noise level and rectify it.

Authors' statement

The authors confirm contribution to the paper as follows: Study conception and design: G.V.A., S.Ch.; Data collection: S.Ch.; Analysis and interpretation of results: G.V.A.; Draft manuscript preparation: G.V.A., S.Ch. The two authors reviewed the results and approved the final version of the manuscript.

Acknowledgements

The author with a deep sense of gratitude would like to thank the supervisor for his guidance and constant support rendered during this research.

References

- Krismer, F. Modelling and optimization of bidirectional dual active bridge DC DC converter topologies. (ETH Zurich, 2010). https://doi.org/10.3929/ethz-a-006395373
- [2] Hartmann, M. Ultra-compact and ultra-efficient three-phase PWM rectifier systems for more electric aircraft. (ETH Zurich, 2011). https://doi.org/10.3929/ethz-a-006834022
- Badstübner, U. Ultra-high performance telecom DC-DC converter. (ETH Zurich, 2012). https://doi.org/10.3929/ethz-a-009777673
- [4] Yin, S., Tseng, K. J., Simanjorang, R., Liu, Y. & Pou, J. A 50-kW high-frequency and high-efficiency SiC voltage source inverter for more electric aircraft. *IEEE Trans. Ind. Electron.* 64, 9124–9134 (2017). https://doi.org/10.1109/TIE.2017.2696490
- [5] Paul, C. R. & Hardin, K. B. Diagnosis and reduction of conducted noise emissions. *IEEE Trans. Electromagn. Compat.* **30**, 553–560 (1988). https://doi.org/10.1109/15.8769
- [6] Wood, R. A. & Salem, T. E. Evaluation of a 1200-V, 800-A all SiC dual module. *IEEE Trans. Power Electron.* 26, 2504–2511 (2011). https://doi.org/10.1109/TPEL.2011.2108670
- [7] Bishnoi, H., Baisden, A. C., Mattavelli, P. & Boroyevich, D. Analysis of EMI terminal modeling of switched power converter. *IEEE Trans. Power Electron.* 27, 3924–3933 (2012). https://doi.org/10.1109/TPEL.2012.2190100
- [8] Fu, D., Wang, S., Kong, P., Lee, F. C. & Huang, D. Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in DC-DC converters. *IEEE Trans. Ind. Electron.* 60, 4968–4977 (2013). https://doi.org/10.1109/TIE.2012.2224071
- [9] Pahlevaninezhad, M., Hamza, D. & Jain, P. K. An improved layout strategy for common-mode EMI suppression applicable to highfrequency planar transformers in high-power DC/DC converters used for electric vehicles. *IEEE Trans. Power Electron.* 29, 1211– 1228 (2014). https://doi.org/10.1109/TPEL.2013.2260176
- [10] Subramanian, A. & Govindarajan, U. Analysis and mitigation of conducted EMI in current mode controlled DC-DC converters. *IET Power Electron.* 4, 667–675 (2019). https://doi.org/10.1049/iet-pel.2018.5322
- [11] Abinaya, A. B. & Magdaline, S. A. Design & Analysis Of Line Impedance Stabilization Network Using RLC Components for ITE. in 2017 International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS) 1–5 (IEEE, 2017). https://doi.org/10.1109/ICIIECS.2017.8275974
- [12] Laour, M. & Tahmi, R. Effective filtering solution with low cost small size for common-mode reduction in dc-dc converters. *Electron. Lett.* 52, 388–390 (2016). https://doi.org/10.1049/el.2015.3296
- [13] Grobler, I. & Gitau, M. N. Conducted EMC Modeling For Accreditation in DC-DC Converters. in *IEEE Industrial Electronics Society (IECON)* 002329–002335 (IEEE, 2015). https://doi.org/10.1109/IECON.2015.7392450
- [14] Chu, Y. & Wang, S. A generalized common-mode current cancelation approach for power converters. *IEEE Trans. Ind. Electron.* 62, 4130– 4140 (2015). https://doi.org/10.1109/TIE.2014.2387335
- [15] Xie, L., Ruan, X. & Ye, Z. Reducing common mode noise in phaseshifted full-bridge converter. *IEEE Trans. Ind. Electron.* 65, 7866– 7877 (2018). https://doi.org/10.1109/TIE.2018.2803761

- [16] Yazdani, M. R., Filabadi, N. A. & Faiz, J. Conducted electromagnetic interference evaluation of forward converter with symmetric topology and passive filter. *IET Power Electron.* 7, 1113– 1120 (2014). https://doi.org/10.1049/iet-pel.2013.0320
- [17] Zhang, Z. & Bazzi, A. M. A virtual impedance enhancement based transformer-less active EMI filter for conducted EMI suppression in power converters. *IEEE Trans. Power Electron.* 37, 11962–11973 (2022). https://doi.org/10.1109/TPEL.2022.3172388
- [18] Zhao, X. et al. Planar common-mode EMI filter design and optimization for high-altitude 100-kW SiC inverter/rectifier system. IEEE Trans. Emerg. Sel. Topics Power Electron. 10, 5290–5303 (2022). https://doi.org/10.1109/JESTPE.2022.3144691
- [19] M'barki, Z., Rhazi, K. S. & Mejdoub, Y. A proposal of structure and control overcoming conducted electromagnetic interference in a buck converter. *Int. J. Power Electron. Drive Syst.* 13, 380 (2022). https://doi.org/10.11591/ijpeds.v13.i1.pp380-389
- [20] Ma, Z., Wang, S., Sheng, H. & Lakshmikanthan, S. Modeling, analysis and mitigation of radiated EMI due to PCB ground impedance in a 65W high-density active-clamp flyback converter. *IEEE Trans. Ind. Electron.* **70**, 12267–12277 (2023). https://doi.org/10.1109/TIE.2023.3239904
- [21] CISPR 25-3. Radio disturbance characteristics for the protection of receivers used on board vehicles, boats and on devices – Limits and methods of measurement. (2018). https://doi.org/10.3403/02771447
- [22] CISPR 25-4. Radio disturbance characteristics for the protection of receivers used on board vehicles. boats and on devices – Limits and methods of measurement. (2014). https://doi.org/10.3403/02771447
- [23] CISPR 25-4. Radio disturbance characteristics for the protection of receivers used on board vehicles. boats and on devices – Limits and methods of measurement. (2016). https://doi.org/10.3403/02771447
- [24] Laour, M., Tahmi, R. & Vollaire, Ch. Modeling and analysis of conducted and radiated emissions due to common mode current of a buck converter. *IEEE Trans. Electromagn. Compat.* 59, 1260–1267 (2017). https://doi.org/10.1109/TEMC.2017.2651984
- [25] Britto, K. R. A., Vimala, R. & Dhanasekaran, R. Modelling of Conducted EMI in Flyback Switching Power Converters. in *IEEE*, *International Conference on Recent Advancements in Electronical*, *Electronics and Control Engineering (ICONRAEeCE)* 377–383 (IEEE, 2011). https://doi.org/10.1109/ICONRAEeCE.2011.6129801
- [26] Mendez, J. B., Freire, M. J. & Prats, M. A. M. Overcoming the effect of test fixtures on the measurement of parasitics of capacitors and inductors. *IEEE Trans. Power Electron.* 35, 15–19 (2020). https://doi.org/10.1109/TPEL.2019.2929209
- [27] Sakurai, T. & Tamaru, K. Simple formulas for two- and threedimensional capacitances *IEEE Trans. Electron. Devices* **30**, 183– 185 (1983). https://doi.org/10.1109/T-ED.1983.21093
- [28] Sohn, Y.-S. Lee, J.-Ch., Park, H.-J. & Cho, S.-I. Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board. *IEEE Trans. Adv. Packag.* 24, 521–527 (2001). https://doi.org/10.1109/6040.982839
- [29] Bogatin, E. Design rules for microstrip capacitance. *IEEE Trans. Components, Hybrids, Manuf. Technol.* 11, 253–259 (1988). https://doi.org/10.1109/33.16649
- [30] Rondon-Pinilla, E., Morel, F., Vollaire, C. & Schanen, J. L. Modeling of a buck converter with a SiC JFET to predict EMC conducted emissions. *IEEE Trans. Power Electron.* 29, 2246–2260 (2013). https://doi.org/10.1109/TPEL.2013.2295053
- [31] Ruchli, A. E. Inductance calculations in a complex integrated circuit. *IBM J. Res. Dev.* 16, 470–481 (1972). https://doi.org/10.1147/rd.165.0470
- [32] Paul, C. R. Inductance: Loop and Partial. (Wiley, Hoboken, 2010).
- [33] Kim, S. & Neikirk, D. P. Compact Equivalent Circuit Model for the Skin Effect. in 1996 IEEE MTT-S International Microwave Symposium Digest 1815–1818 (IEEE, 1996). https://doi.org/10.1109/MWSYM.1996.512297
- [34] González-Vizuete, P., Bernal-Méndez, J. & Martín-Prats, M. A. Reducing conducted emissions at the output of full-bridge DCDC converters with high voltage steps. *Electronics* 10, 1373 (2021). https://doi.org/10.3390/electronics10121373
- [35] Weens, Y., Idhir, N., Bausiere, R. & Franchaud, J. J. Modeling and simulation of unshielded and shielded energy cables in frequency and time domains. *IEEE Trans. Magn.* 42, 1876–1882 (2006). https://doi.org/10.1109/TMAG.2006.874306