BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES, Vol. 72(1), 2024, Article number: e148839
DOI: 10.24425/bpasts.2024.148839

DC power supply with parallel active compensation function and tuneable inductive filter based on analogue control: Part 1

Michał GWÓŹDŹ and Łukasz CIEPLIŃSKI*

Poznan University of Technology, Faculty of Control, Robotics and Electrical Engineering, Piotrowo 3A, 60-965 Poznan, Poland

Abstract. In this paper, a DC power supply is presented that, in addition to a power factor correction, is equipped with an active power filter function. This function enables compensation of both the reactive and the distortion power, generated by an external load, which is connected to the same power line node as the presented device. A tuneable inductive filter is added at the input of the power electronics controlled current source, which constitutes the main block of the power supply. This filter allows for a visible improvement in the quality of the current source control, compared to a similar device with a fixed inductive filter. This improvement depends on extending the "frequency response" of the current source, which facilitates an increase in the dynamics of changes in the input current of the power supply. The actual modification to the presented device is related to its control section, which is equipped with analogue regulators. The main purpose of this work is to present the results from a simulation model of an electrical system with a power supply, especially compared to those from a similar device but with a discrete control. The work represents a continuation of a research cycle on DC power supplies that are equipped with a power compensation function and are based on tuneable magnetic devices.

Keywords: active compensator; analogue control; power factor correction; DC power supply; tuneable inductive filter.

1. INTRODUCTION

The current work forms part of a research project on DC power supplies with both a power factor correction (PFC) and a shunt active power filter (SAPF) function, based on a tuneable magnetic device [1, 2].

The negative impact of nonlinear loads on the operation of the power grid is widely known and is a well-analysed problem (see e.g. [3–7]). For example, solutions with diode and thyristor rectifiers and simple power electronics converters draw a distorted current and this is the main reason for their negative impact on the operation of the power grid. The most essential elements of this impact are an increase in power loss, a reduction in the capacity of the power line, and the generation of electromagnetic disturbances. A further effect is the reduction in the lifetime of both the power line itself and the other loads, connected to it, including those which do not negatively impact the operation of the power line. In addition to its purely technical effects, this problem needs to be considered in terms of its economic and social impacts (e.g. in terms of health). Hence, various kinds of compensators, mainly in the form of passive and active filters, are used in electrical systems as a preventive measure. The main task of these devices is to ensure appropriate mapping of the shape of the current at its input to the shape of the current that is drawn from the power line node by the other loads connected to it. As a result of this compensation process, the total current, drawn from the power line node, should have both a suitable shape and a suitable phase relation with the voltage waveform in the power line node, depending on the power compensation strategy used (see e.g. [8–11]).

The subject of this paper is a DC power supply (PSP) with a PFC and additional SAPF function. In the power electronics voltage-controlled current source (VCCS), which is the main component of the PSP structure, a tuneable inductive filter is used [12]. This solution represents a novel approach to these devices. Furthermore, the control section of the PSP is equipped with analogue regulators, facilitating the extended frequency response of the VCCS. As a result of these modifications, the quality of the compensation process is improved, compared to typical solutions based on SAPFs.

It is worth noting here that analogue control of the converter output quantity (current, voltage) is widely used by manufacturers of integrated circuits (ICs), designated for energy conversion/energy management tasks, in the low/medium-power range, based on AC/DC, DC/DC, and DC/AC converters, which use a few main topologies. The analogue solutions there give good technical and economical results. The leading companies in this field are Analog Devices Inc. and Texas Instruments, which design and manufacture modern ICs, based on its know-how. The numerous descriptions of the devices with analogue control, manufactured by worldwide companies, can be found on their websites, in the form of application notes, white papers, data sheets, and circuits-from-the-labs documents [13, 14].

The following sections of this paper describe: the principle of operation of the DC power supply, the impact of the system

*e-mail: lukasz.cieplinski@put.poznan.pl

Manuscript submitted 2023-06-08, revised 2023-09-05, initially accepted for publication 2023-11-28, published in February 2024.

parameters on the dynamics of the VCCS, the principle of operation of a tuneable inductive filter, the purpose of using analogue regulators, and the results from a simulation model test of an electrical system with the PSP. The last section presents some conclusions.

2. STRUCTURE OF A DC POWER SUPPLY

The concept of a DC power supply, operating with PFC and a SAPF function, equipped with a tuneable inductive filter, was presented in previous work [1] and only a brief explanation of the structure of a PSP and the rules of its operation is given in this section for the reader's convenience.

A block diagram of an electrical system with a PSP is shown in Fig. 1. An assumption is made that this system is based on a single-phase power line, and the block denoted as "other loads" is not taken into account.

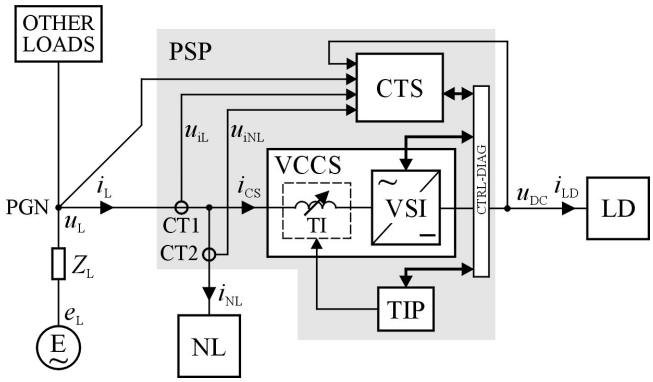

Fig. 1. Block diagram of an electrical system including a DC power supply, equipped with both a PFC and a compensation function

The system consists of the following main components:

- E – power source in the line.
- PGN – power grid node with internal impedance Z_L.
- PSP – DC power supply. The PSP consists of several internal blocks: the VCCS, the power stage of the tuneable inductive filter (TIP block), and two current transducers (CT1, CT2). The CTS is the PSP control section, which is interconnected with both the voltage source inverter (VSI) and the TIP, via the control-diagnostics bus (CTRL–DIAG). The CTS block operates based on the following external signals: u_L, $u_{iL} = i_L r_{CT}$, $u_{iNL} = i_{NL} r_{CT}$, and u_{DC}, where r_{CT} is the transfer factor of the current transducers.
- NL – nonlinear load, connected to the same power line node as the PSP.
- LD – load, connected to the DC link of PSP.

As a result of the entire compensation process, the total current (i_L), drawn from the power line node, should have both a suitable shape and a suitable phase relation with the voltage waveform in the grid node, depending on the chosen compensation strategy [9]. In this paper, Fryze's power theory [15] was chosen for control of the compensation function of the PSP. In this theory, the VCCS generates a suitable distorted current (i_{CS}) which, when combined with the current of the nonlinear load, results in (theoretically) a sinusoidal total current (i_L), drawn from a power line node, as follows:

$$i_L(t) = i_{NL}(t) + i_{CS}(t) = i_{ref,L}(t) = I_{ref,I} \sin(\omega_L t), \qquad (1)$$

where $I_{ref,I}$ is the amplitude of the reference signal and ω_L is the frequency of the voltage in the power line.

2.1. Impact of the system parameters on the dynamics of the VCCS

The input power stage of the PSP consists of an inductive filter (L_{CS}) and H-type transistor bridge (Fig. 2), which form the VCCS [16, 17]. The primary task of this block is to provide a voltage (u_{DC}), with the required value, to the DC link of the PSP. The second task is to compensate for both the phase shift and the higher harmonics of the current, drawn by the nonlinear load (NL). The inductive filter increases the value of the input impedance of the current source and minimises the magnitude of the PSP input current, associated with the pulse modulation carrier signal (PWM here), which is used to control the VSI [17].

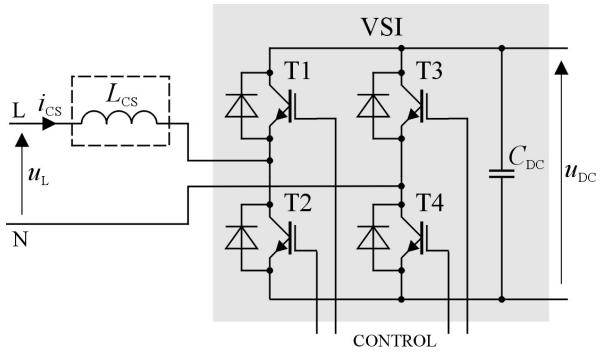

Fig. 2. Diagram of the input power stage of PSP, VCCS

Taking into account the linear model of the VCCS [1, 17] it is assumed that during the given half-periods of the line voltage waveform the appropriate pairs of transistors (T1–T4 or T3–T2) are turned on. The VCCS input current waveform is then described by the following general formula (However, it does not include: the inductive filter resistance, power line impedance, and voltage drops at the switches in the VSI.):

$$i_{CS}(t) = \frac{1}{L_{CS}} \int [u_{DC} - |u_L|] \, dt, \qquad (2)$$

where L_{CS} is the filter inductance.

The ability of the VCCS to shape the PSP input current is mainly determined by the value of its bandwidth (BW), i.e. the frequency response. For a linear model of the VCCS, the value of is determined by the following formula:

$$BW = \frac{1}{2\pi I_{CS}} SR, \qquad (3)$$

where I_{CS} is the magnitude of the VCCS input current, and SR is the slew-rate parameter for this current [1, 18].

Based on the assumptions made here, the value of SR results directly from the value of the first derivative of the VCCS input current waveform, given by (2), and hence:

$$SR = \frac{u_{DC}(t) - \left|U_L \sin(\omega_L t)\right|}{L_{CS}}, \tag{4}$$

where U_L is the line voltage amplitude.

The value of the SR parameter then depends on the instantaneous value of the DC voltage, the instantaneous value of the line voltage, and the inductance of the filter in the VCCS block. Thus, the SR parameter reaches two extreme values, which are given by the equation as follows:

$$SR_{min} = \left.\frac{[u_{DC}(t_i) - U_L]}{L_{CS}}\right|_{t_i=\left(\frac{1}{2}+i\right)\frac{\pi}{\omega_L}:\ i=0,\pm1,\pm2,\ldots}, \tag{5}$$

$$SR_{max} = \left.\frac{u_{DC}(t_i)}{L_{CS}}\right|_{t_i=i\frac{\pi}{\omega_L}:\ i=0,\pm1,\pm2,\ldots}. \tag{6}$$

From (5) and (6) it can be seen that the VCCS has the narrowest bandwidth (SR = SR_{min}) when the instantaneous value of the line voltage reaches its maximum and the widest bandwidth (SR = SR_{max}) when the voltage in the power line passes through zero.

Since the values of both the grid voltage and the voltage in the DC link of the PSP are set in advance, the only quantity that can increase the dynamics of the changes in the VCCS input current is a reduction in the filter inductance; however, this directly results in an increase in the magnitude of the PWM carrier component in the PSP input (and the power line) current. Hence, in order to increase the frequency response of the current source, the use of a filter with a variable value of inductance is proposed. This solution allows for a better approximation of the PSP input current shape to the "ideal" waveform (which exists only theoretically), imposed by (1), in relation to a VCCS, equipped with a fixed inductive filter. At the same time, when the system is operating in the "steady state", the magnitude of the pulse modulation carrier component in the DC power supply input current remains at the minimum assumed level.

2.2. Tuneable inductive filter

The details of the whole modelling procedure for the filter and its implementation in the VCCS have also been presented in previous papers [1,2] and only a brief description of this device is given in this section.

In a tuneable inductive filter, the phenomenon of coupling between a pair of magnetic fluxes is exploited (see Fig. 3).

The reactance (X_{TI}) of the inductive filter, seen from the power source side (u_1), has two values, that are dependent on the state of the S-switch:

$$X_{TI} = \left(1 - s_{T\text{–}TI}k^2\right) X\Big|_{s_{T\text{–}TI}=0 \vee s_{T\text{-}TI}=1}, \tag{7}$$

where X, assuming $L_1 = L_2 = L$, is the own reactance of the coil, k is the magnetic coupling coefficient of the coils, $s_{T\text{–}TI} = 0$

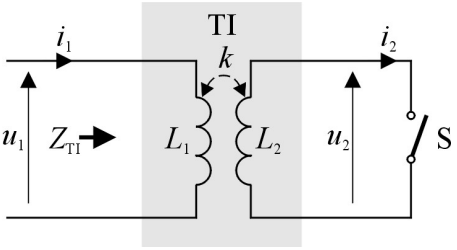

Fig. 3. Diagram showing basic operation of a tuneable inductive filter

represents the S-switch in the open state, and $s_{T\text{–}TI} = 1$ represents the S-switch in the closed state.

The simulation model of the inductive filter is based on a three-winding transformer with a ferromagnetic core, equipped with a working air gap [1,2].

The assumed reactance ratio for the filter, related to both states of the S-switch, is defined as:

$$x_{S\text{-}TI} = \frac{X_{TI}\big|_{s_{T\text{–}TI}=0}}{X_{TI}\big|_{s_{T\text{–}TI}=1}}, \tag{8}$$

and should be equal to approximately three. A further assumption was made that the value of the filter inductance (L_{TI}), in both states of the S-switch, should be in the range 1–5 mH. These values were chosen based on the results of PSP simulation studies, as a compromise between a possible increase in the VCCS frequency response and minimisation of the magnitude of the PWM carrier components in the PSP input current. For these assumed values for the parameters the inductance of the filter, in both states of the S-switch, was equal to 4.52 mH and 1.51 mH.

2.3. Tuneable inductive filter and TIP block

The details of the interconnection between the filter and the TIP block are shown in Fig. 4.

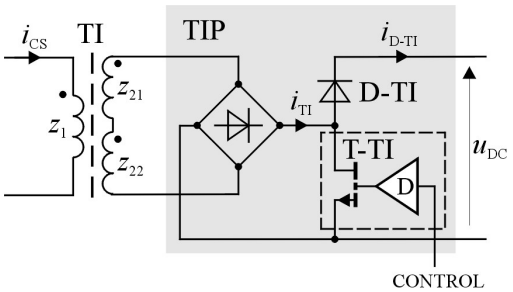

Fig. 4. Diagram showing the inductive filter and TIP block, where the D block is the driver of the T-TI transistor

The key role here is played by the aforementioned three-winding transformer with split secondary windings, to which a fast rectifier bridge was attached. The output of the rectifier is connected to the drain of the T–TI transistor (the S-switch) and the negative rail of the DC-link of the PSP. This configuration for this circuit has an advantage in that the energy, associated with the leakage flux (collected in TI after T–TI is turned on),

is then passed to the DC-link of the PSP (after T–TI is turned off), which facilitates a reduction in the power loss in both TI and TIP.

3. PURPOSE OF USING ANALOGUE REGULATORS

Unlike the use of analogue signal processors, digital technology offers almost unlimited possibilities in terms of designing control algorithms, for diverse types of objects, (e.g. [19, 20]). Programming techniques also allow for the design of control system solutions that can dynamically adapt the values of their parameters to the changing values of external conditions. The high quality of operation of these algorithms, as mathematical functions, depends on the high accuracy of signal processing by digital methods and the main limitation of these methods is the resolution of the mathematical units of the processor. Hence, the market share of μP and μC systems is increasing, since these operate on a floating-point system of numerical notation that guarantees an extremely high accuracy of mathematical operation. Nevertheless, in the context of an overall assessment of the quality of the digital algorithm performance, both the analogue front-end of the control system and the analogue-to-digital conversion process should be respected too [21, 22]. Numerous articles have explored, both qualitatively and quantitatively, the negative impact of the effects of the signal sampling process on the quality of operation of the algorithm, which is related to the essence of this process as well as the nature of analogue signals (e.g. [23–25]). The most important of these effects are related to the non-stationarity of the signal sampling block (LTV – Linear Time Variant class of objects) and the almost inevitable phenomenon of aliasing of signal spectra, which results in a partial loss of the information, carried by the sampled signal. A negative impact on the operation of the system may also arise from the error, introduced by each analogue-to-digital converter (ADC), in the form of the so-called quantisation noise [19, 20, 26].

At the level of the transfer function of a digitally implemented two-port network, it is noted that this differs from the transfer function of its analogue prototype in terms of the magnitude and phase parts of the transfer function (e.g. [23–25]). Thus, if this digital component is an element in a closed feedback loop for an automatic control system, the impact on the stability of the system of the additional time delay, introduced by this component into the signal flow path, should be considered. This delay results not only from the implementation in the ADC (typically with a successful approximation register architecture – SAR) of the sample-and-hold block but also from the construction of the mathematical function itself, at the level of the signal flow graph [22, 24, 27]. An additional effect of the sampling process that is often overlooked by researchers and designers is the modification of the transfer function of the digital two-port network, in relation to its analogue prototype, which also contains aliases of the transfer function of this prototype. These aliases affect the size of the stability margin for the entire closed feedback loop system [23–25, 27, 28]. For this reason, digital algorithms have certain imperfections, which affect the quality of the device operation to a greater or lesser extent. In the case of the PSP control system, the reason for a potential solution for its control section in analogue form is the possibility of achieving higher precision in the control of the VCCS input current shaping process (as indicated by the results of theoretical analyses [27, 28]), in relation to a "purely" digital control. Especially, in the transient states of this current, highly dynamic changes in its value are seen. The higher precision of control arises from the inherent dynamic limitations of both signal sampling and signal processing, which apply to any real μP-based control system. Theoretically, it is possible to further increase a signal conversion rate by the ADC (in this case, related to the conversion of the feedback signal mainly, u_{iL}, see Fig. 1). However, one negative consequence of this is a need for the higher computing power of the control system, meaning that the expected cost of the system will increase. Given the assumed value of the technical profit, understood here as the degree of improvement in the quality of the VCCS input current (and the power line current), this may cause economic problems. Another significant advantage of an analogue regulator, compared to a digital solution, is the possibility of increasing the value of its effective gain, while maintaining the stability of the operation of the system [27, 28]. This is a direct effect of the elimination of the aforementioned time delays from the analogue signal path. When the gain of the regulator is increased, the quality of the entire control process also increases, in terms of a higher quality of mapping of the output quantity (here, the VCCS input current) to the reference signal. As a result, the value of the control error (ε_{REGI}), defined in (9), can be minimised:

$$\varepsilon_{REGI} = \sqrt{2}\frac{\overline{|u_{err,I}|^2}}{U_{ref,I}}\,100\%, \tag{9}$$

where, as shown in the diagram of the REGI block (see Fig. 5), $u_{err,I} = u_{ref,I} - u_{iL}$ is the error signal, related to the VCCS current regulator block and $U_{ref,I}$ is the amplitude of the reference signal for this block.

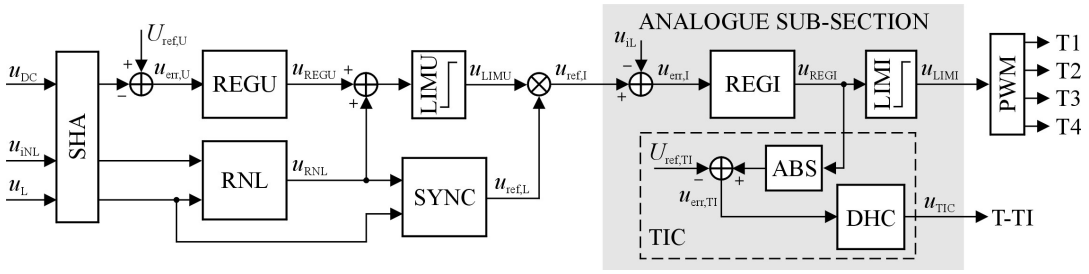

Fig. 5. Diagram of the control section (CTS) of the PSP simulation model

4. PSP SIMULATION MODEL

To confirm the correctness of the initial assumptions made here, in terms of both the topology of the PSP and the rules of its operation, a simulation model of an electrical system with this device was created. The model was built in the OrCAD/PSPICE environment.

The tests conducted with this model focused on three main aspects of its operation:

- Verification of the structure and parameter values of the tuneable filter control block (TIC) and its power stage (TIP).
- Verification of the structure and parameter values of the analogue current regulator (REGI), in the context of possible further minimisation of the control error value.
- Development of guidelines for the future design of a laboratory prototype of the system with PSP.

4.1. The power stage of the PSP

The power stage of the simulation model of the VCCS was designed with ready-to-use components, available from the ORCAD library. The values of their basic, static, and dynamic parameters, were modified based on catalogue data for an IPM/IGBT device (type PM50RLA120, manufactured by Mitsubishi Electric [29]). As a physical prototype of the T–TI simulation model, the LMG3425R030 power module with a JFET GaN transistor, manufactured by Texas Instruments, was chosen, [30]. The reason for using this component was the high expected value of the switching speed for T–TI. The components of the system in Fig. 4, indicated with a dashed line, form a part of the internal structure of this module. In addition to the power transistor itself, the module contains the driver for the transistor (D block) and is equipped with protection functions for the transistor. In this case, for modelling purposes, also only the basic catalogue parameters of the LMG3425R030 were considered. Both of the aforementioned power devices are planned to be used in a future implementation of a laboratory model of the power supply. As the model of the tuneable inductive filter, the "XFORM_linear" component from the ORCAD library was used.

4.2. Control section of the PSP

A block diagram of the PSP control section (CTS) is shown in Fig. 5. The current version of the PSP simulation model includes, among other parts, two regulators and a tuneable inductive filter control block, as follows:

- SHA – This is a sample-and-hold amplifier(-s) block that is related to the digital part of the control system.
- REGU – This is the (master) voltage regulator in the DC link of the PSP, which operates at both the reference signal $U_{\mathrm{ref,U}}$ and the DC voltage; this regulator affects the value of the reference signal amplitude ($u_{\mathrm{ref,I}}$), which is related to the REGI block. A P-type REGU was chosen.
- RNL – This is the block for calculating the current value of the active power of the nonlinear load. Its operation is based on Fryze's power theory; the summation node for REGU and RNL blocks adds two active powers: AC load power and DC load power (related to the NL and LD blocks, respectively). Both the REGU output signal (u_{REGU}) and the RNL output signal (u_{RNL}) are step functions of time, i.e. with a constant value in each half-period of the reference signal ($u_{\mathrm{ref,L}}$).
- LIMU – This is the limiter of the sum of output signals from the REGU and RNL blocks (u_{REGU} and u_{RNL}, respectively). It imposes a maximum value on the VCCS input current, in the context of the catalogue parameters (mainly current limitations) of the physical IPM/IGBT module.
- REGI – This is the analogue current regulator, and a diagram of this block is shown in Fig. 6.

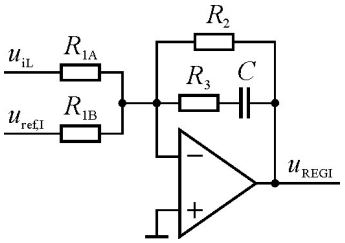

Fig. 6. Diagram of the REGI block

The REGI operates based on the sum of the reference signal ($u_{\mathrm{ref,I}} = u_{\mathrm{LIMU}} u_{\mathrm{ref,L}}$) and the feedback signal (u_{iL}), where $u_{\mathrm{ref,L}}$ is a unity-amplitude sinusoidal signal that is phase-synchronised with the grid voltage, i.e. $u_{\mathrm{ref,L}} = \sin(\omega_{\mathrm{L}} t)$ [17, 31, 32].

The REGI transfer function, expressed in terms of values of the components shown in Fig. 6, is as follows:

$$T_{\mathrm{REGI}}(\mathrm{j}\omega) = k_{\mathrm{REGI}} \frac{\mathrm{j}\dfrac{\omega}{\omega_{\mathrm{REGI,2}}} + 1}{\mathrm{j}\dfrac{\omega}{\omega_{\mathrm{REGI,1}}} + 1}, \tag{10}$$

where (assuming $R_{1A} = R_{1B} = R_1$) $k_{\mathrm{REGI}} = -\dfrac{R_2}{R_1}$ is the gain of REGI for DC, $\omega_{\mathrm{REGI,1}} = \dfrac{1}{(R_2 + R_3)C}$, and $\omega_{\mathrm{REGI,2}} = \dfrac{1}{R_3 C}$ are the characteristic frequencies (1 and 2, respectively) of (10).

The REGI block operates based on the sum of the two input signals, as follows:

$$U_{\mathrm{REGI}}(\mathrm{j}\omega) = T_{\mathrm{REGI}}(\mathrm{j}\omega)\left[U_{\mathrm{iL}}(\mathrm{j}\omega) + U_{\mathrm{ref,I}}(\mathrm{j}\omega)\right]. \tag{11}$$

The model of the amplifier, used in the REGI, was based on a precision, wideband, "rail-to-rail input & output" operational amplifier type ADA4806-1, manufactured by Analog Devices Inc. [33–35].

- LIMI – This is the limiter of the magnitude of the REGI output signal, which protects the PWM block against an over-modulation.
- PWM – This block is responsible for generation of the PWM signal.
- TIC – This is the tuneable filter control block, as shown in Fig.5. The elements of the TIC block are the ABS block (which calculates the absolute value of the REGU output signal), the summing node (which compares the value of the output voltage from ABS with the reference signal for the TIC block), and the comparator with a dynamic hysteresis

loop (DHC block) [36, 37], a diagram of which is shown in Fig. 7.

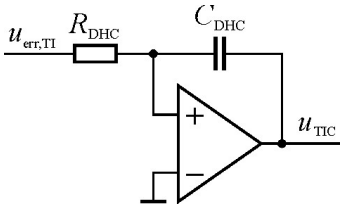

Fig. 7. Diagram of the DHC

The DHC operates based on the signal $u_{\mathrm{err,TI}} = |u_{\mathrm{REGI}}| - U_{\mathrm{ref,TI}}$. If $u_{\mathrm{err,TI}} > 0$ the output of the comparator goes to a high state and the T–TI switch is turned on. The DHC (unlike a static comparator) provides a certain minimum value of pulse duration at its output, which is related to its time constant, $\tau_{\mathrm{DHC}} = R_{\mathrm{DHC}} C_{\mathrm{DHC}}$ [37]. As a result, the maximum value of frequency of such pulses, generated in a series by DHC, is limited too. This feature is important for proper control of the T–TI transistor, in terms of not exceeding its catalogue dynamic limitation. This results in both a reduction in the power loss in the T–TI device and an increase in the resistance of the PSP control system to electromagnetic disturbances.

5. TEST RESULTS FROM THE SIMULATION MODEL

The operating conditions of the system were close to the nominal ones, and the power of the NL block was set to 50% of the PSP-rated output power. The non-linear load block was a thyristor voltage regulator with a thyristor firing angle of 90°, loaded with a resistor. This kind of load generates almost a step change in the power line current, with a significant magnitude, thus, it imposes extremely high requirements on the desired dynamics of the changes in the VCCS input current (i_{CS}), see Fig. 8. These conditions of the NL block operation are well suited for evaluating the quality of operation of PSP as an active power filter.

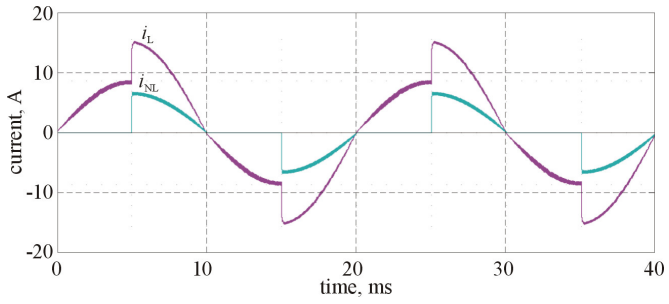

Fig. 8. Current waveforms in the model with the power compensation function of the PSP disabled

The basic quantities, used to characterise the quality of the i_{L} current, were: the normative total harmonic distortion coefficient (THD), the total waveform distortion coefficient (TWD) [38–40], the duration of the transient state in this current (τ_{L}), after a step change in the value of the NL block current, and the value of the control error ($\varepsilon_{\mathrm{REGI}}$), which is related to the operation of the current regulator (REGI). In the first part of these tests the voltage in the DC-link of the PSP was set to its nominal value, see Table 1.

Table 1
Main parameters of the simulation model

No.	Parameter	Symbol	Value
Rated parameters of the model			
1	RMS grid voltage	$U_{\mathrm{L,RMS}}$	230 V
2	Grid voltage frequency	f_{L}	50 Hz
3	Grid impedance	R_{L}	0.63 Ω
4	Rated output power of the PSP	$P_{\mathrm{DC,nom}}$	1.2 kW
5	DC bus nominal voltage and its setting range	$U_{\mathrm{DC,n}}$	375 ± 25 V
6	Maximum magnitude of the PSP input current	–	13.5 A
Parameters of the VCCS			
7	Inductance of TI: S-switch open	L_{TI}	4.52 mH
8	Inductance of TI: S-switch closed	L_{TI}	1.51 mH
9	Capacitor in the DC bus	C_{DC}	1 mF
10	PWM carrier frequency	f_{c}	10 kHz
Parameters of the voltage regulation block			
11	Sampling frequency (SHA block)	f_{s}	10 kHz
12	REGU gain	k_{REGU}	0.25
13	LIMU signal limiting level	$A_{\mathrm{L,U}}$	±15 V
Parameters of the VCCS current control block			
14	REGI gain	k_{REGI}	2000
15	REGI characteristic frequency (1)	$f_{\mathrm{REGI,1}}$	76 Hz
16	REGI characteristic frequency (2)	$f_{\mathrm{REGI,2}}$	1.59 kHz
17	REGI signal limiting level	$A_{\mathrm{L,I}}$	±500 V
Parameters of tuneable inductive filter control block			
18	DHC time constant	τ_{DHC}	2 $upmu$s
19	Signal reference value for DHC	$U_{\mathrm{ref,TI}}$	490 V

The value of THD for the NL block current (i_{NL}) was 64.3%, while the value of THD for the DC power supply input current (i_{L}) was 21.2%.

Figure 9 in turn shows the PSP input current, in its transition state, together with the T–TI control signal, for three different values of τ_{DHC}.

Reducing the DHC time constant to below 2 μs no longer resulted in a visible improvement in the degree of mapping of the PSP input current in the reference signal for REGI. In addition, the resolution of the T–TI switch control signal became too small above a value of 7–8 μs to improve the shape of this current. So, the test results, presented in the following correspond to a DHC time constant of 2 μs, unless stated otherwise.

In Fig. 10 the waveforms of a reference signal for REGI ($u_{\mathrm{ref,I}}$), PSP input current (i_{L}), and NL block current (i_{NL}), for

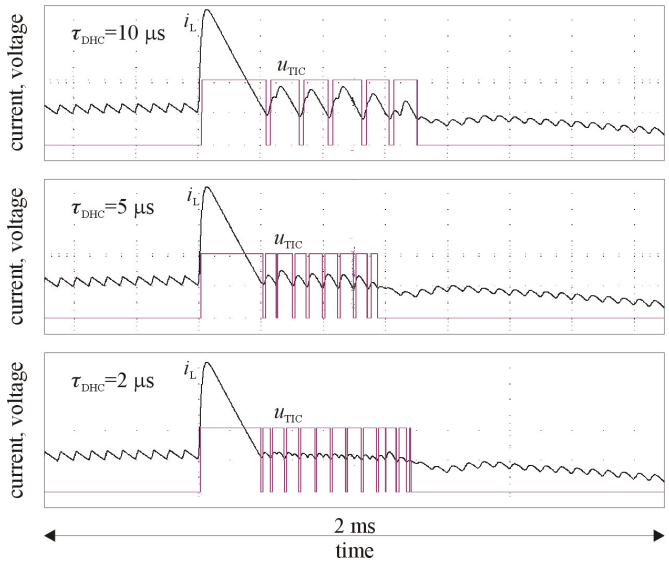

Fig. 9. Graphs of the DC power supply input current waveform and the T–TI control signal for DHC time constants of 10, 5, and 2 μs

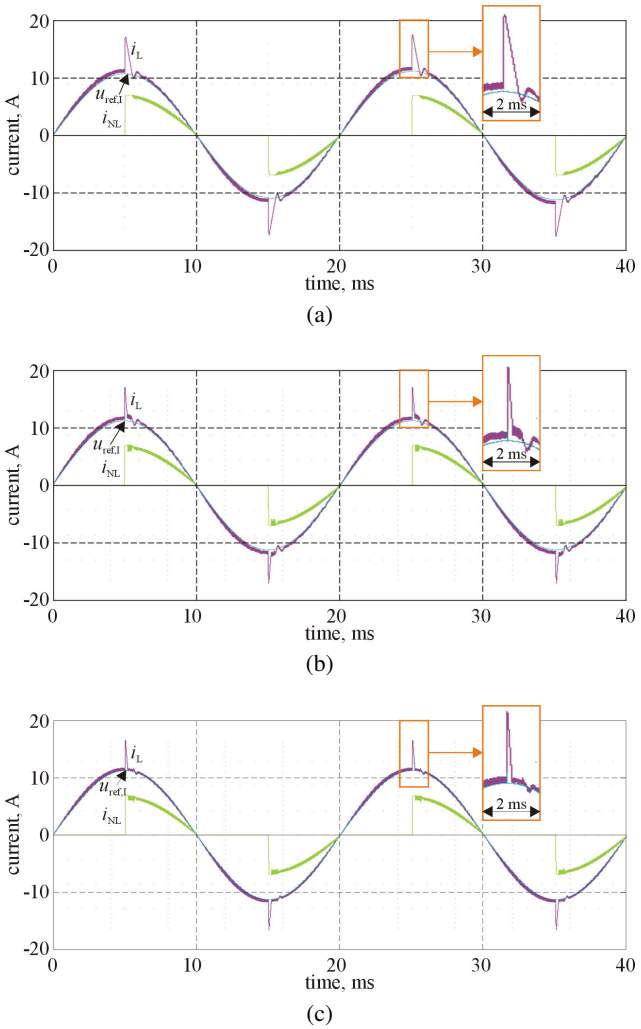

Fig. 10. Voltage and current waveforms for the simulation model of the PSP with the power compensation function activated, for three variants of VCCS: (a) FFDC, (b) TFDC, and (c) TFAC

three variants of the VCCS block and the PSP control section configuration are presented, i.e.: FFDC (fixed inductive filter and discrete control), TFDC (tuneable inductive filter and discrete control), and TFAC (tuneable inductive filter and analogue control).

Figure 11 shows the spectrum envelope for the waveforms of the PSP input current (i_L), which is presented in Fig. 10. The use of a tuneable inductive filter in the VCCS allowed for reduction up to the 50th harmonics of the PSP input current (i.e. in the 2.5 kHz band). The analogue version of the control section allowed for further minimisation of these harmonics, in relation to discrete control.

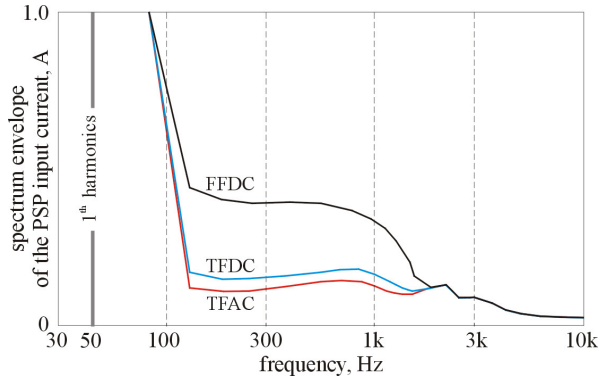

Fig. 11. Spectrum envelope for the PSP input current, corresponding to the current waveforms in Fig. 10

Figure 12 presents the results of the next part of the tests, in the form of the curves for: TWD, τ_L, and ε_{REGI}, for the PSP input current (i_L) vs. the DC voltage ($\overline{u_{DC}}$), in terms of changes in this voltage, given in Table 1. These tests indicated that with the analogue control section, the values of TWD and ε_{REGI} for the DC power supply were significantly reduced to 71% and 50% on average, respectively, compared to discrete control. In the case of ε_{REGI}, a clear improvement in the quality of the DC power supply current was seen, due to the much higher value (approximately 2.5 times) of the gain-bandwidth product (GBP) of the analogue regulator, compared to the digital version, under conditions of system stability [27, 28]. However, analogue control did not result in a visible reduction in the value of τ_L, in relation to discrete control. The test results showed that lowering the value of the time constant for the DHC below a certain minimum had no further effect in terms of shortening the duration of the transient state in the input current of the VCCS. The reasons for this state of affairs are two-fold, existing the non-zero filter own time constant and, to a lesser extent, the non-zero value of the power grid impedance. Another reason, although of lesser importance, is the nature of the pulse response of the chosen topology current regulator. In each of the cases presented here, the quality of operation of the DC power supply as SAPF increased with an increase in the voltage in the DC link, which is consistent with (5) and (6). In light of these formulas, the obvious conclusion is that for sufficiently high voltage in the DC circuit, the sense of using a tuneable inductive filter becomes questionable. This statement was confirmed by the laboratory experiments [2].

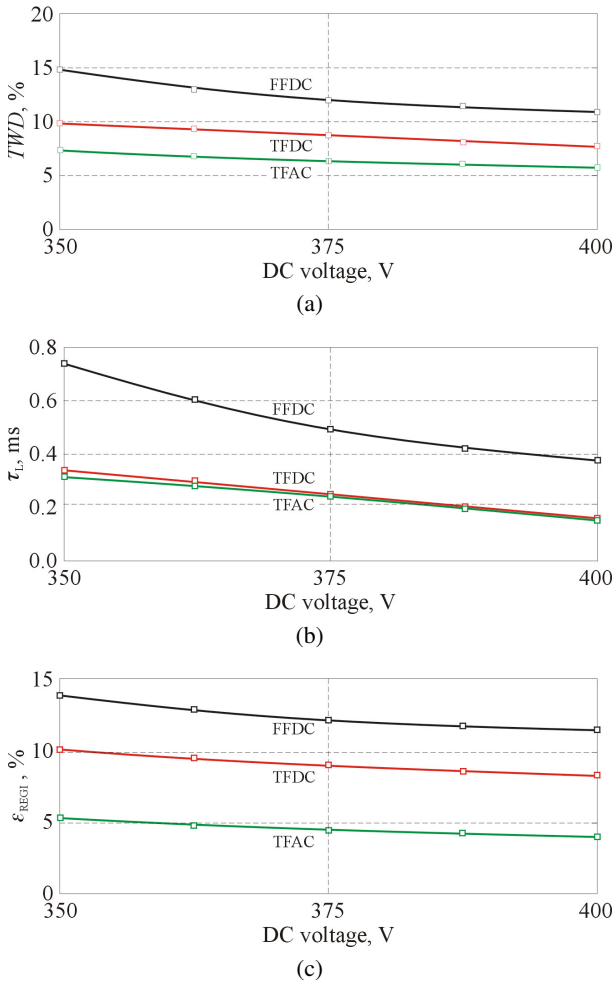

Fig. 12. Curves of (a) TWD, (b) τ_L, and (c) ε_{REGI} vs. the DC voltage in the PSP, for different variants of the VCCS control section

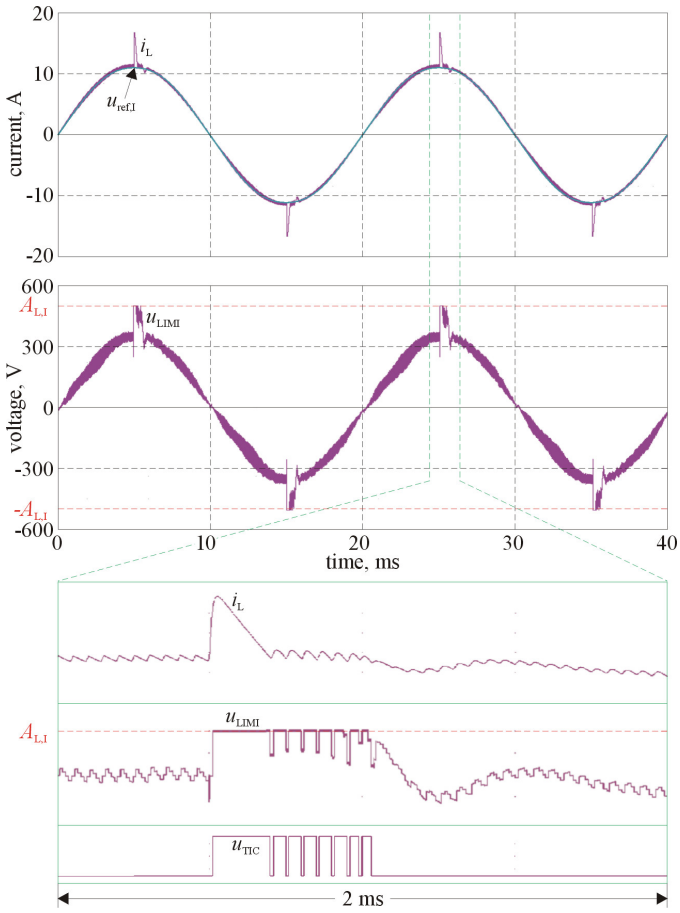

Fig. 13. Waveforms from the simulation model for a transient state of the PSP input current, showing the REGI output signal and PSP input current with the T–TI control signal, for $\tau_{DHC} = 5$ µs

Figure 13 shows the details of the REGI output signal and the PSP input current waveforms, together with the S-switch (the T–TI transistor) control signal. These waveforms represent the response of the simulation model to a step change in the NL block current.

The nature of the obtained waveforms indicates that in a state of saturation of the output of the REGI, the DHC block takes over its role, becoming a follow-up regulator with high dynamics of operation.

6. CONCLUSIONS

The tests of the simulation model of the DC power supply, equipped with an analogue control section, were conducted and its results were compared with those from a similar device that was equipped with a discrete control. These results showed that two of the three key parameters of the DC power supply (TWD and ε_{REGI}), which were used to assess the quality of its operation, were significantly improved with analogue control as compared to digital control. However, the third parameter (τ_L) was not visibly improved. This was due to naturally occurring dynamic constraints on the operation of the PSP, related mainly to the own time constants of the inductive filter in both states of the S-switch.

Based on the results from these PSP simulation model tests, achieving similar control effects with the use of a fully digital system needs increasing (even in a noticeably obvious way) the required computation power of the processor in the PSP control section. This solution could therefore become economically unjustified. The use of an additional element in the form of a GaN module may also result in a certain increase in the cost of the PSP. However, in a possible three-phase version of the PSP, this module could be a common control device for a three-phase variant of tuneable inductive filter. This possibility was indicated by the results of theoretical considerations and simulation studies, regarding the method of controlling the inductive filter in a three-phase version of the power supply [12]. LMG3425R030 module, which is planned for implementation in a future laboratory prototype of the power supply, has the integrated functions necessary to ensure the reliable operation of the GaN transistor. The expected increase in the cost of the prototype of the power supply would therefore be relatively low.

Based on the state-of-the-art of analogue microelectronics devices (e.g. [13, 14]) "purely" analogue solutions are not suitable for application in complex control systems for technical reasons,

including, e.g. adaptive regulators, which were exemplified in the previous paper [41].

REFERENCES

[1] M. Gwóźdź, Ł. Ciepliński, and M. Krystkowiak, "Power supply with parallel reactive and distortion power compensation and tunable inductive filter – Part 1," *Bull. Pol. Acad. Sci. Tech. Sci.*, vol. 68, no. 3, pp. 401–408, 2020, doi: 10.24425/bpasts.2020.133383.

[2] M. Gwóźdź, R. Wojciechowski, and Ł. Ciepliński "Power supply with parallel reactive and distortion power compensation and tunable inductive filter – Part 2," *Bull. Pol. Acad. Sci. Tech. Sci.*, vol. 69, no. 4, 2021, doi: 10.24425/bpasts.2021.137938.

[3] G. Benysek and M. Pasko, *Power Theories for Improved Power Quality*, Springer-Verlag, London, 2012.

[4] H. Akagi, E.H. Watanabe, and Aredes M., *Instantaneous Power Theory and Applications to Power Conditioning*, John Wiley & Sons: 408 Hoboken, NJ, USA, 2017; ISBN: 9781118362105.

[5] M. Pasko, D. Buła, K. Dębowski, D. Grabowski, and M. Maciążek, "Selected methods for improving operating conditions of three-phase systems working in the presence of current and voltage deformation – Part I," *Arch. Electr. Eng.*, vol. 67, pp. 591–602, 2018.

[6] X. Qiao, J. Bian, C. Chen, and H. Li, "Comparison and analysis of reactive power compensation strategy in power system," *Proceedings of the 2019 IEEE Sustainable Power and Energy Conference (iSPEC)*, Beijing, China, 2019, pp. 689–692, doi: 10.1109/iSPEC48194.2019.8975301.

[7] L. Czarnecki and M. Almousa, "Adaptive balancing by reactive compensators of three-phase linear loads supplied by nonsinusoidal voltage from four-wire lines," *Am. J. Electr. Power Energy Syst.*, vol. 10, pp. 32–42, 2021, doi: 10.11648/j.epes.20211003.11.

[8] H. Akagi, A. Nabae, and S. Atoh, "Control Strategy of Active Power Filters Using Multiple vol.tage – Source PWM Converters," *IEEE Trans. Ind. Appl.*, vol. 22, no. 3, pp. 361–368, 1977.

[9] A. Teke, M. Meral, and M. Tumay, "Active Power Filter: Review of Converter Topologies and Control Strategies," *Gazi University Journal of Science*, vol. 24, no. 2, pp. 283–289, 05.04.2011.

[10] T. Adrikowski, D. Buła, and M. Pasko, "Selection of method for reactive power compensation and harmonic filtering in industrial plant," *2017 Progress in Applied Electrical Engineering (PAEE)*, 2017, pp. 1–5, doi: 10.1109/PAEE.2017.8009010.

[11] L. Czarnecki, "Currents' physical components (CPC) – based power theory a review. Part I: power properties of electrical circuits and systems," *Przegląd Elektrotechniczny*, vol. 95, no. 10, pp. 1–11, 2019.

[12] M. Gwóźdź, "Power electronics active shunt filter with controlled dynamics," *Compel-Int. J. Comp. Math. Electr. Electron. Eng.*, vol. 32, no. 4, pp. 1337–1344, 2013.

[13] "Power Management," Analog Devices Inc., [Online]. Available: https://www.analog.com/en/product-category/power-management.html [Access: 01.09.2023].

[14] "Power Management," Texas Instruments Inc., [Online]. Available: https://www.ti.com/power-management/overview.html [Access: 01.09.2023].

[15] S. Fryze, "Active, reactive, and apparent power in circuits with nonsinusoidal voltage and current," *Przegląd Elektrotechniczny*, vol. 13, pp. 193–203, 1931.

[16] M.P. Kaźmierkowski, R. Krishnan, and F. Blaabjerg, *Control in Power Electronics Selected Problems*, Academic Press Series in Engineering Book, 2003.

[17] M.H. Rashid, *Power Electronics Handbook*, Elsevier Ltd. Oxford, ISBN: 0-12-581650-2, 2018.

[18] S. Bolkowski, *Theory of electric circuits*, WNT, Warszawa, 2007. (in Polish)

[19] J. Bentsman, *Introduction to Signal Processing, Instrumentation, and Control, An. Integrative Approach*, World Scientific Publishing: Singapore, 2016.

[20] S. Stergiopoulos, *Advanced Signal. Processing Handbook: Theory and Implementation for Radar, Sonar, and Medical Imaging Real Time Systems, Electrical Engineering & Applied Signal*, Processing Series, 1st ed., CRC Press: Boca Raton, FL, USA, 2000.

[21] W. Kester, *The Data Conversion Handbook*, Analog Devices Inc., Newnes, 2005.

[22] V.K. Madisetti, *The Digital Signal Processing Handbook*, vol. 3, Set, CRC Press: Boca Raton, FL, USA, 2010.

[23] B. Francis and T. Georgiou, "Stability theory for linear time-invariant plant with periodic digital controllers," *IEEE Trans. Autom. Control*, vol. 33, no. 9, pp. 820–832, 1988.

[24] L. Mirkin, "Transfer functions of sampled-data systems in the lifted domain," *Proc. 44th IEEE Conf. on Decision and Control & European Control Conf. ECC'05* (Seville, Spain), 2005, pp. 5180–5185.

[25] M. Gwóźdź, "Stability of Discrete-Time Systems on Base of Generalized Sampling Expansion," *Proc. XXXIV Conference ICSPETO 2011*, Gliwice-Ustoń, Poland, 2011, pp. 71–72.

[26] J. Borkowski, D. Kania, and J. Mroczka, "Influence of A/D quantization in an interpolated DFT based system of power control with a small delay," *Metrol. Meas. Syst.*, vol. 21, pp. 423–432, 2014.

[27] J.C. Doyle, B.A. Francis, and A.R. Tannenbaum, *Feedback Control Theory, Dover Publications,* 2013.

[28] T. Kaczorek, A. Dzieliński, W. Dąbrowski, and R. Łopatka, *Fundamentals of control theory*, Warszawa, WNT, 2020. (in Polish)

[29] "Intelligent Power Modules" Mitsubishi Electric, [Online]. Available: http://www.mitsubishielectric.com/semiconductors/products/powermod/intelligentpmod/index.html [Access: 07.06.2023].

[30] "LMG3425R030," Texas Instruments Inc., [Online]. Available: https://www.ti.com/product/LMG3425R030 [Access: 07.06.2023].

[31] W. Jarzyna, "A survey of the synchronization process of synchronous generators and power electronic converters," *Bull. Pol. Acad. Sci. Tech. Sci.*, vol. 67, pp. 1069–1083, 2019.

[32] M. Gwóźdź and Ł. Ciepliński, "An Algorithm for Calculation and Extraction of the Grid voltage Component," *Energies*, vol. 14, no. 16, p. 4842, 2021, doi: 10.3390/en14164842.

[33] "Op Amp Subtleties, section XI," Analog Devices Inc., [Online]. Available: https://www.analog.com/media/en/training-seminars/design-handbooks/Amplifier-Applicatons-Guide/Section11.pdf [Access: 07.06.2023].

[34] "Rail-to-Rail Op Amps," Analog Devices Inc., [Online]. Available: https://www.analog.com/en/product-category/rail-to- rail-op-amps.html [Access: 07.06.2023].

[35] "ADA4806-1," Analog Devices Inc., [Online]. Available: https://www.analog.com/en/products/ada4806-1.html [Access: 07.06.2023].

[36] J.M. De la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey," *IEEE Trans. Circuits Syst. I-Regul. Pap.*, vol. 58, no. 1, pp. 1–21, Jan. 2011, doi: 10.1109/TCSI.2010.2097652.

[37] M. Gwóźdź, "Power Electronics Programmable vol.tage Source with Reduced Ripple Component of Output Signal Based on Continuous-Time Sigma-Delta Modulator," *Energies*, vol. 14, no. 20, p. 6784, 2021, doi: 10.3390/en14206784.

[38] M.H.J. Bollen and I.Y.H. Gu, *Signal Processing of Power Quality Disturbances*, Wiley-IEEE Press: Piscataway, NJ, USA, 2006.

[39] IEC Standard, IEC 61000-2-2: Environment-Compatibility Levels for Low-Frequency Conducted Disturbances and Signalling in Public Low-voltage Power Supply Systems, International Electrotechnical Commission (IEC); IEC: Geneva, Switzerland, 2002.

[40] A. Arranz-Gimon, A. Zorita-Lamadrid, D. Morinigo-Sotelo, and O. Duque-Perez, "A Review of Total Harmonic Distortion Factors for the Measurement of Harmonic and Interharmonic Pollution in Modern Power Systems," *Energies*, vol. 14, p. 6467, 2021, doi: 10.3390/en14206467.

[41] D. Matecki and M. Gwóźdź, "Programmable Broad-Band Power Electronics Current Source with GaN Transistors in Power Stage," *Progress in Applied Electrical Engineering (PAEE)*, Kościelisko, Poland, 2018, pp. 1–5, doi: 10.1109/PAEE.2018.8441156.