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A novel edge computing approach to astronomical image data processing based on sCMOS camera using SoC

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***Abstract*—The ever-growing deluge of astronomical data challenges traditional server-based processing, hindering real-time analysis and scientific discovery. This paper proposes a novel approach: edge computing directly on an sCMOS camera using a System-on-Chip (SoC) architecture currently developed at Creotech Instruments. We present a custom-designed camera equipped with an FPGA-based SoC, enabling on-board pre-processing and feature extraction of astronomical images. This significantly reduces data transmission, minimizes latency, and empowers real-time decision-making for critical observations. We showcase the camera's capabilities through real-world scenarios, demonstrating its usability in astronomy.**

***Keywords*—sCMOS camera; astronomical camera; Space Surveillance and Tracking (SST); FPGA; edge computing; SoC**

I. INTRODUCTION

CREOTECH Instruments boasts a rich heritage in crafting intricate control and measurement systems, encompassing advanced camera solutions. Our contributions to pioneering projects like the Pi of the Sky at Las Palmas Observatory, ASOPEK for the Air Force Institute of Technology's SST telescope, and Neostel for ESA, stand as testaments to our unwavering pursuit of innovation. This drive to push boundaries extends to esteemed collaborations with CERN, GSI, CCFE, LNLS, and more, where we've participated in the development of cutting-edge control and measurement systems for High Energy Physics applications.

While working on the development of new generations of astronomical cameras, we noticed the following two emerging trends:

- Emerging Power of sCMOS Sensors: Scientific CMOS (sCMOS) sensors are rapidly evolving, offering performance comparable to leading-edge CCD sensors while necessitating less cooling and consuming less energy. This makes sCMOS technology a highly Jerzy attractive alternative for a wide range of applications.
- Increasing the amount of data generated by astronomical cameras when large area sCMOS sensors are used allowing for much faster readout speeds than CCDs. While CCD sensors operated at speeds on the order of single frames per second, sCMOS offer an increase to the level of tens.

Modern astronomical cameras, equipped with powerful sCMOS sensors, capture vast amounts of information with exceptional detail. This surge in data volume, while enabling groundbreaking discoveries, poses significant challenges for traditional data processing and storage infrastructures. Addressing these data-driven hurdles is crucial for maximizing the scientific return of next-generation astronomical observations.

The still-growing generation of data has not only an economic impact but is leaving a significant environmental footprint. The constant transfer and storage of information require massive energy consumption, primarily from data centers fueled by fossil fuels. While efficient technologies are emerging, addressing the climate impact of data necessitates collective action. From optimizing data storage and utilizing renewable energy sources to promoting responsible data consumption, tackling this challenge requires a multifaceted approach to ensure a sustainable digital future.

The emergence of high-sensitivity, high-resolution sCMOS cameras with rapid frame rates presents exciting opportunities for advanced astronomical and SST applications. However, the substantial data streams generated by these sensors pose infrastructure challenges.

In response, we propose a novel camera architecture that integrates high-performance sCMOS sensors with the on-board computational power of advanced FPGA SoC-based electronics. This enables real-time, on-camera data pre-processing, significantly reducing data volume and enhancing overall system efficiency.

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Furthermore, for applications demanding fast feedback and control, the camera can function as an autonomous trigger source, leading to a dramatic reduction in response times. This inherent autonomy is particularly advantageous in distributed systems, making our solution highly relevant for SST applications and beyond.

An attempt to address the above challenges using a newly developed astronomical camera using a high-speed, high-resolution sCMOS sensor and SoC chip, along with the results of tests conducted and plans, is described in the following sections of this article.

II. SOC ARCHITECTURE CONCEPT

Like any measurement device, an astronomical camera consists of a sensor, in the case we are discussing, an sCMOS, and a unit that allows data acquisition, in our case an SoC chip. Because of the use of a state-of-the-art sCMOS sensor, it is not necessary to use discrete ADCs or analog front ends, as they are built into the sensor and the data transmitted by the sensor is in digital form. It is also necessary to control the sensor, but for this article, we will not go into its details. The overview of such configuration is depicted in Figure 1. It should be emphasized that the 6k x 6k resolution sCMOS sensor presented in the demonstrator can generate tens of gigabits per second of image data. The challenge, therefore, is not only to serve it, but also to make it usefully available to other systems.

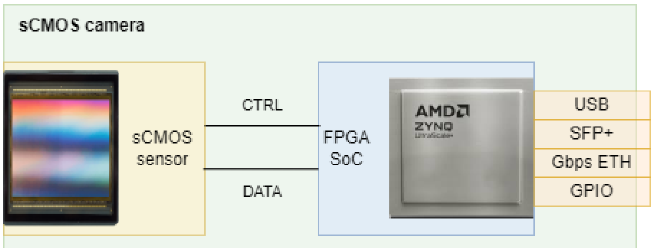

Fig.1. The overview of the camera readout architecture

The presented AMD Zynq Ultrascale+ SoC also offers possibility to communicate with external devices with multiple interfaces, such as:

- USB 3.0 in device mode, USB 2.0 in host mode
- 10GbE connected through SFP+ enabling easy integration with storage and control servers using fibre optical link
- Classical 1Gbps ethernet for separate management, diagnostics etc.
- General Purpose I/O lines that can be configured as for example incoming and outcoming triggers

The SoC used in the described camera is running Linux on the Cortex A53 cores.

The platform is a very versatile base for building autonomous control and measurement systems and implementing real-time data processing algorithms, including those using machine learning. Within the framework of this article, two examples of such implementations are presented: one for data reduction through frame stacking to accelerate further processing of SST data, and a demonstrator of a control and measurement system based on the described solution.

III. EXAMPLE IMPLEMENTATION OF IMAGE STACKING

We will use image frame stacking as an example of implementing edge computing functionality. This is a basic activity performed when processing data from astronomical cameras, but it requires significant resources in terms of both operating memory and computing unit performance. If this operation is performed already on the camera, the optimization of the object detection process is significant and easy to convert into saved transfer, storage space, and computational time. It also saves invaluable time, because by performing it in real-time, we get the unique ability to react quickly.

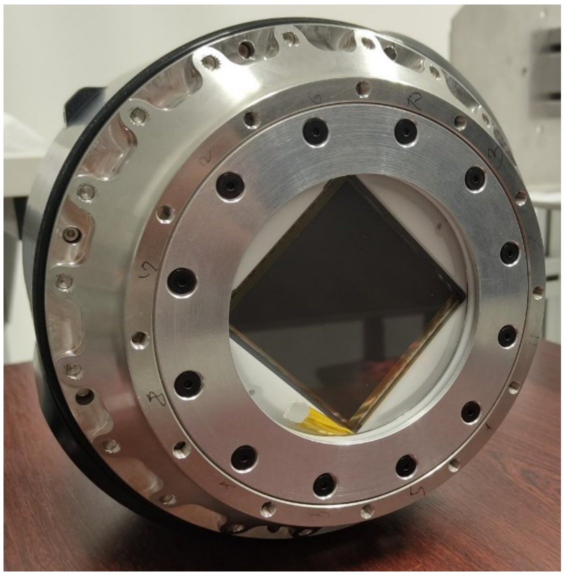

Fig.2. CreoSky 6000 camera, photo with visible large area sCMOS sensor

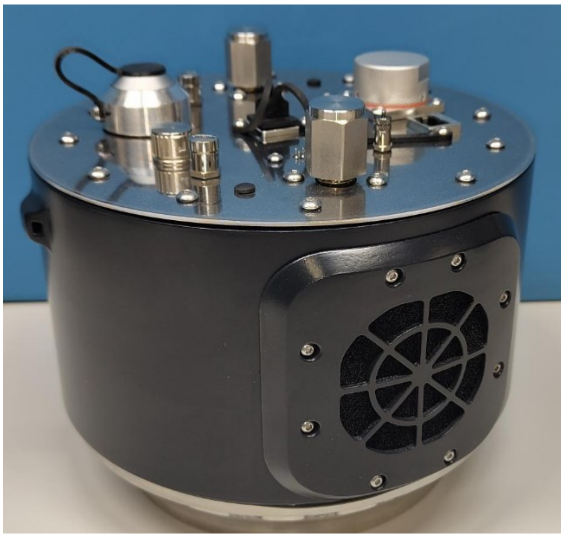

Fig.3. CreoSky 6000 camera with IO ports visible

All demonstrations presented are implemented using the CreoSky 6000 camera from Creotech Instruments. This device is equipped with an sCMOS sensor with a resolution of 6k x 6k pixels and a maximum reading speed of 22FPS. Each frame takes up over 70MB of memory. The camera is presented in images 2 and 3.

The camera architecture is based also on the Xilinx FPGA. The IP block for data processing implemented in the FPGA section provides the user with the ability to perform operations on the collected photos in real-time. Although the module is under development, it provides, among other things, the ability to stack photos or subtract frames from each other. The algorithm is fully configurable from the Linux application via configuration registers. An example of the data processing path is shown in figure 4. The presented algorithm enables the automatic stacking of up to 16 frames in the FPGA on the fly without any significant performance or latency penalties.

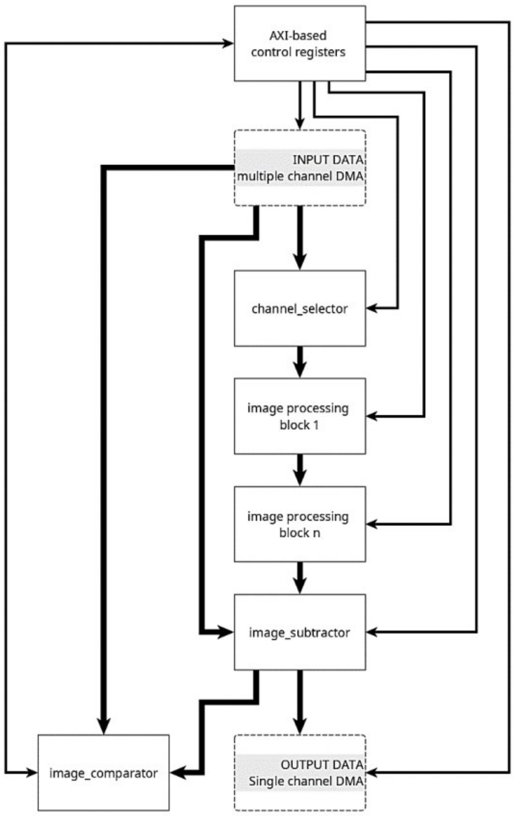

Fig.4. Example of the data processing with simple stacking path

This architecture leverages a modern, advanced System-on-Chip (SoC) integrating an application processor and Field-Programmable Gate Array (FPGA) on a single chip. This enables several key advantages:

- Low-latency, in-situ data processing: Data can be processed directly on the camera, minimizing latency and improving responsiveness.
- Future-proof machine learning capabilities: The FPGA allows for hardware acceleration of both software-based and intellectual property (IP) core-based machine learning algorithms, ensuring adaptability to future advancements. This feature is described in more detail in the following chapters of this article due to potential confusion for readers unfamiliar with the Zynq Ultrascale+ platform
- Hard real-time data processing: The FPGA's inherent parallelism facilitates deterministic, high-speed data processing crucial for real-time applications.
- Easy algorithm prototyping in Linux userspace: The open-source Linux environment empowers rapid development and testing of new algorithms directly on the camera.

The presented in Figure 4 simple algorithm of multi-frame stacking can save multiples of the frame size. A simple calculation can lead to the conclusion that stacking 2 frames can lead to saving more than 70MB of transfer and data storage (1 frame size), 4 frames increase the number to 210MB (3 frames), and with 16 frames stacked we only send about 70MB instead of more than 1GB. The correctness of data acquisition and calculations performed are reflected in the charts presented in Figures 5, 6, 7, 8, 9, and 10.

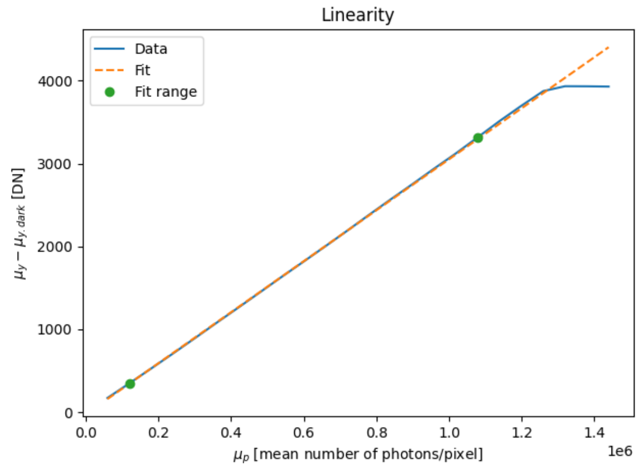

Fig.5. 12bit LN mode Linearity plot

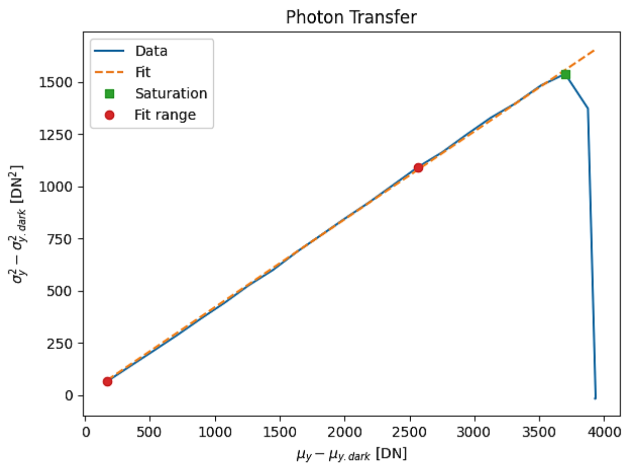

Fig.6. 12bit LN mode Photon Transfer plot

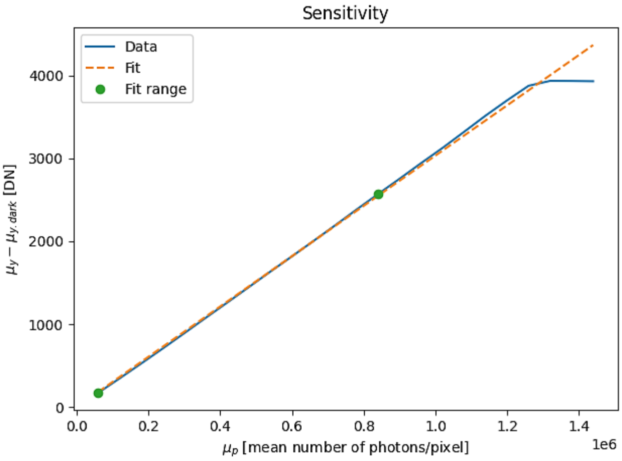

Fig.7. 12bit LN mode Sensitivity plot

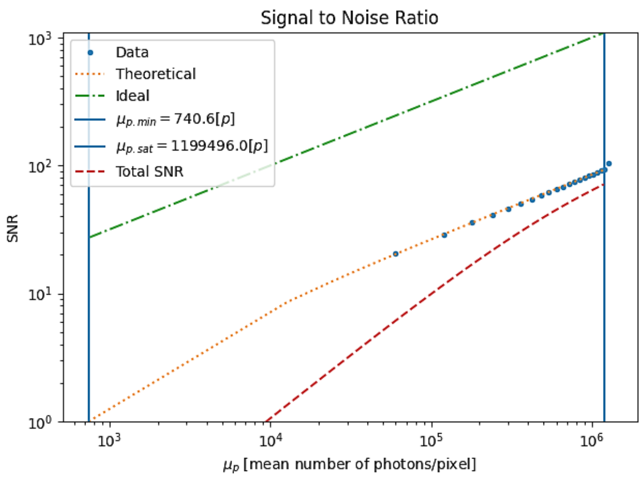

Fig.8. 12bit LN mode SNR plot

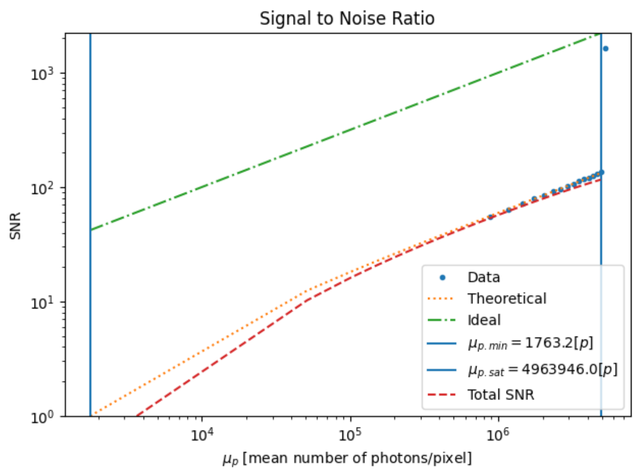

Fig.9. 12bit LN mode SNR plot for two image stack

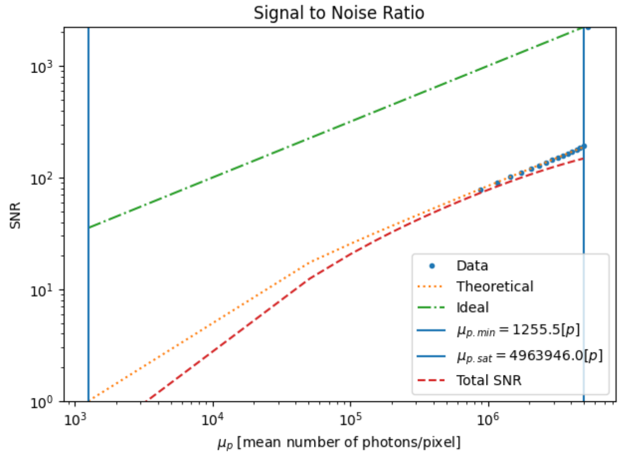

Fig.10. 12bit LN mode SNR plot for four image stack

The presented charts confirm not only the correct operation of the algorithm, but also the expected increase in dynamics. This is because when averaging frames, the impact of noise on the received signal is reduced, which is another advantage of using this type of algorithms. Deviations from the ideal may result from the cosmetics of the sensor, which in grade engineering samples may contain many defects and affect the results obtained.

From the results of the verification process, we can also conclude that the developed and implemented architecture together with the specific algorithm does not cause disruptions in the operation of the very demanding data acquisition path from the sCMOS sensor.

The presented static method of implementing image data processing algorithms can be extended with machine learning. This is possible thanks to the tools and programming libraries provided by Xilinx, along with unique fragments enabling ML acceleration in FPGA. The overview of this solution is presented in figure 11.

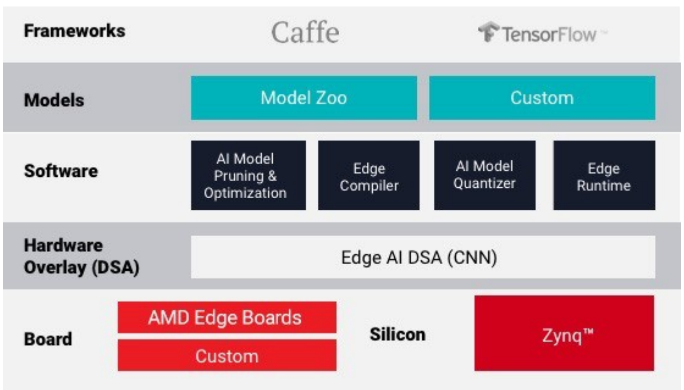

Fig.11. AMD Zynq machine learning acceleration solution overview [7]

This machine learning-based solution has not yet been tested with the CreoSky 6000 camera but is an interesting subject of further development conducted in cooperation with scientific and research units specializing in either astronomy or computer science.

Another interesting and potentially groundbreaking solution in astronomy and astronomical data processing could be the use of solutions that go even further. One of them is AMD Pynq, potentially allowing the implementation of Machine Learning in the very popular Python language without the knowledge of coding in HDL or knowledge of FPGA, while using the acceleration they offer. The overview of this solution is presented in the figure 12.

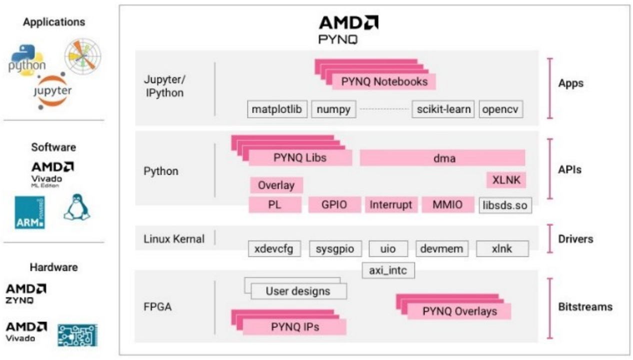

Fig.12. AMD Zynq machine learning - Pynq solution overview [7]

Further work on the implementation of embedded processing is planned soon. Sadly, circumstances beyond the control of the project contractors accompanying its implementation made it impossible to carry out the tests on time. Currently, these tests are being organized, and as soon as they are carried out, they will result in obtaining new knowledge and opportunities allowing for further progress in the presented solutions.

IV. sCMOS CAMERA IN REAL-TIME CONTROL SYSTEM

As mentioned earlier, advanced real-time data processing algorithms not only allow for the reduction of data sent by the device to external systems or their processing time but also provide a unique opportunity to build real-time control and measurement systems enriched with very sensitive, high-resolution optical sensors. and imaging speed. The schematic diagram of the Camera demo can be found in the figure 12.

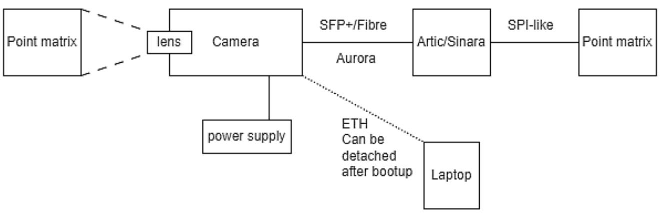

Fig.12. EQTC real-time demo schematic diagram

To demonstrate the uniqueness of the developed solution, a demonstrator was built enabling imaging of a matrix of points simulating the atoms of a quantum computer, image processing, and then sending very low-latency digital data to the control system. In this case, the system connected to the camera via optical fiber controlled an identical matrix of points. This allowed for empirical demonstration of the unique ability of the CreoSky 6000 device to operate deterministically in real-time. In this case, the camera read the sensor in row-skip mode at a speed of about 300 times per second, and data processing and sending took no more than 3 nanoseconds. On the other side of the optical fiber, the Kasli SOC controller of a very popular set of quantum computer control tools - Artiq/Sinara - was connected. The image of the demonstrator taken during the EQTC conference is presented in the figure 13.

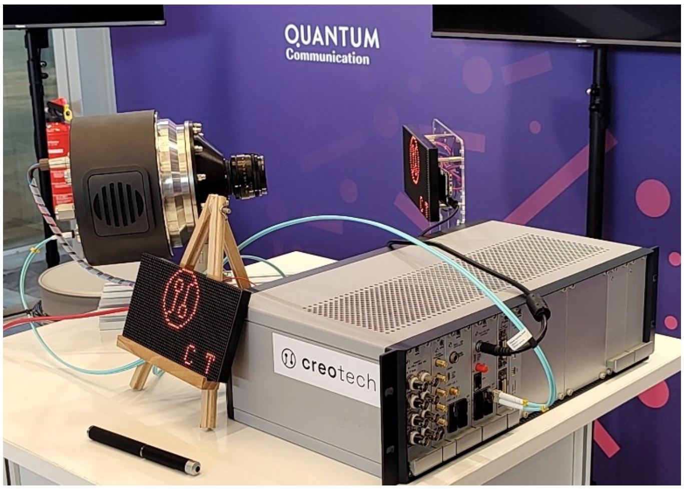

Fig.13. EQTC real time demo photo presenting CreoSky 6000 camera with accompanying systems

The demonstrator was not only a technical success but also aroused considerable interest among conference participants.

The algorithm implemented in the demonstrator used the previously described architecture. Instead of stacking frames, he divided the image into segments identifying individual points pretending to be atoms of a quantum computer and then, by averaging the values for the area, classified the area as in the excited state or not. The architecture of multi-stream image processing together with the possibility of parameterizing the algorithm enabled the easy construction of a control and measurement system.

This type of possibility of both hardware and software reconfiguration depending on the application is unique on the market. Apart from purely utilitarian values, it also offers significant scientific potential in a very dynamically developing area - machine learning.

V. CONCLUSION

The results obtained are very promising and further work in the direction outlined in this article is more than justified. Unfortunately, the Sars-Cov-2 pandemic caused long-term delays and made it impossible to conduct a test campaign using a real telescope. Currently, these tests are being organized, and as soon as they are carried out, their results will be used to improve the described solutions.

The innovative camera design discussed in this paper is currently in the Final Prototype Model phase of development. Initial characterization results indicate the correctness of the assumed architecture and design. Currently, there are advanced discussions with prospective clients interested in the product.

The CreoSky 6000 camera, outlined in this paper, is designed for flexibility and modularity, allowing for seamless integration of various sensor types, and enabling novel applications. One such application is being explored in the QuantEra project "New Imaging and Control Solutions for Quantum Processors and Metrology," conducted in collaboration with partners from Max-Planck-Institut für Quantenoptik and the Institute of Physics, Zagreb. This project focuses on developing a camera tailored to the requirements of quantum technologies, applied in specific use cases such as improving efficiency and reducing qubit state readout time in quantum computers (critical for error correction) and enhancing the short-term stability of hybrid atomic clocks. Moreover, the camera is slated for use in microscopy and spectroscopy applications in biology and chemistry.

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