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EFFECT OF Cu-Cu HYBRID BONDING HEIGHT IN THE 3D STACKED DIE CONFIGURATION: THERMAL-STRUCTURAL ANALYSIS

Advanced packaging technologies, such as Intel's Embedded Multi-Die Interconnect Bridge and Foveros, have revolutionized semiconductor integration by enabling compact, high-performance devices through 3D stacked die configurations. This study focuses on the warpage effects in 3D stacked die configurations using copper-copper (Cu-Cu) hybrid bonding under thermal cyclic conditions, which are critical for ensuring semiconductor device reliability. The research employs ANSYS simulations through Thermal-Structural Coupling to analyze temperature distribution, thermal strain, and Von-Mises stress across different Cu-Cu hybrid bonding heights. Findings indicate uniform heat transfer across thermal cycles, with significant stress concentrations at corner bonding interfaces. Reducing Cu-Cu hybrid bonding height from 0.025 mm to 0.017 mm mitigates thermal strain and stress, with the 0.017 mm height proving optimal for minimizing warpage effects. This research provides insights crucial for enhancing semiconductor packaging reliability. It addresses industry demands for energy-efficient and compact electronic devices and supports industry standards, cost-efficiency, and innovation in semiconductor engineering.

Keywords: Hybrid bonding; Thermal-Structural Coupling; Warpage; 3D stacked die; Thermal cycles

1. Introduction

The increasing demand for smaller, more functional, and efficient electronic devices has pushed semiconductor packaging to evolve rapidly. As Moore's Law approaches its limits, creating smaller yet more powerful chips has become increasingly challenging, driving the need for innovative approaches [1,2]. Integrated Circuit (IC) packaging has undergone significant advancements, shaped by technological progress, enhancement in surface mount technology and the push for higher performance. Surface Mount Technology (SMT) offers various packaging options for diverse applications. These include the versatile Small Outline Package (SOP), the compact Shrink Small Outline Package (SSOP), the ultra-thin Thin SOP (TSOP) for smart cards, and the Quad Flat Package (QFP) with gull-wing leads on all sides. Chip Size Packaging (CSP) and Ball Grid Array (BGA) further expand packaging possibilities, enabling higher integration and efficiency in modern electronics [3].

Advanced packaging technologies address increased integration, performance, and size reduction demand. Fan-out wafer-level Packaging (FOWLP) redistributes I/O connections for compact designs and improved performance. Wafer-level chip-scale Packaging (WLCSP) packages semiconductor dies directly on the wafer, reducing package size. Chiplet-based packaging integrates multiple chiplets within a single package, promoting design flexibility. 3D IC Packaging stacks semiconductor dies using through-silicon vias (TSVs) for vertical integration. System-in-Package (SiP) integrates multiple components into a single package for modular solutions. Embedded Wafer-Level Ball Grid Array (eWLB) embeds the ball grid array directly, simplifying manufacturing and enhancing performance. Flip-Chip Ball Grid Array (FCBGA) flips the semiconductor die for direct substrate connection, improving electrical performance and heat dissipation. These technologies represent significant advances in miniaturization and performance enhancement of electronic devices [4-6].

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EMIB (Embedded Multi-Die Interconnect Bridge) and Foveros are advanced packaging technologies developed by Intel to integrate multiple chips into a single package. EMIB is a packaging technology that enables the integration of multiple chips or dies with a high-density interconnect bridge embedded in the package to optimize overall system performance. Foveros is a 3D packaging technology developed by Intel that allows for vertically stacking multiple chips and connecting through through-silicon vias (TSVs) [7]. It enables the creation of three-dimensional chip architectures, providing benefits such as reduced footprint, improved power efficiency, and enhanced performance. It allows for stacking chips with different technologies and functions while promoting flexibility in design.

In semiconductor engineering, 3D stacked die configurations using Cu-Cu direct advanced packaging have opened new opportunities while posing significant challenges [8]. The push for more powerful, energy-efficient, and compact devices has driven the need to go beyond traditional 2D packaging. Cu-Cu direct technology enables vertical stacking of semiconductor dies in tight spaces, boosting computational power. However, this advancement also brings complex thermal-structural interactions, leading to warpage and reliability issues [9]. By unravelling the complexities of thermal behaviours, fluid dynamics, and structural implications, this study seeks to provide insights crucial for ensuring the reliability and longevity of semiconductor devices using thermal-structural analysis. The pivotal role of thermal cyclic research in 3D stacked die configurations of Cu-Cu direct advanced packaging technology becomes evident in its contribution to industry standards, cost savings, innovation, support for high-stakes applications, and the continual evolution of technology.

2. Methodology

The 3D geometry of the Cu-Cu direct advanced package is created using SolidWorks, and the thermal cyclic chamber model is developed using Design Modeler in ANSYS. A grid independence test is carried out to reduce discretization error. Subsequently, the material properties and boundary conditions are set up for the model. This study focuses on a single Cu-Cu hybrid bonding height design parameter.

2.1. Mathematical equations

The heat transfer of radiation in this simulation is the S2S radiation model. It computes the radiation exchange within an enclosure consisting of gray-diffuse surfaces. The interaction between any two surfaces is influenced by their size, distance, and relative orientation. These parameters are calculated by a geometric function called a "view factor" [10]. The governing equations of the S2S model are shown below:

$$q_{out,k} = \epsilon_k \sigma T_k^{\,4} + (1-\epsilon_k) q_{in,k} \tag{1}$$

Where, $q_{out,k}$ isenergy flux leaving the surface k, ϵ_k is an emissivity of surface k, σ is a Boltzmann's constant, T_k is the absolute temperature of surface k, $q_{in,k}$ is energy flux incident on the surface k.

$$q_{in,k} = \sum_{j=1}^{N} F_{kj} q_{out,k}$$

then

$$q_{out,k} = \epsilon_k \sigma T_k^{\,4} + (1-\epsilon_k) \sum_{j=1}^{N} F_{kj} q_{out,k}$$

Which can be written as:

$$J_k = E_k + (1-\epsilon_k) \sum_{j=1}^{N} F_{kj} J_j \tag{2}$$

Where, J_k is aradiosity of surface k, E_k is emitted radiation of surface k, F_{kj} is a view factor between surface k and surface j, and J_j is a radiosity of surface j.

For forced convection, fluid motion is generated by fans rather than by buoyancy forces. The governing equations for forced convection are based on the principles of mass conservation, momentum, and energy [11,12].

2.2. Computational approach

The 3D geometry of the package is created using Solidworks, as shown in Fig. 1 and imported to the ANSYS FLUENT [13]. Then, the thermal cyclic chamber model was developed using the ANSYS Design Modeler. The chamber was modeled with heaters, a fan, and the imported package (Fig. 2). For the fluid domain, the complete chamber geometry replicates the actual chamber with dimensions of 410 × 280 × 300 mm. The chamber was equipped with a fan featuring five blades. The blades had a thickness of 1 mm and a diameter of 95 mm. The position and direction of the fan are set at the right corner and negative y-axis, respectively, since the air blown by the fan flows through the holes in the negative y-axis. The heater was installed at the center of the top side, while the package was positioned in the middle of the fluid domain. The dimensioning and number of parts for the package are shown in TABLE 1.

The material properties for the package assembly were sourced from previous research studies [14,15] and the ANSYS material database. These properties were subsequently assigned within the fluid and structural analysis computational setup.

The air density is set as an incompressible ideal gas for material properties to model the fluid motion driven by density variations due to temperature differences. The heater was assigned the thermal cyclic test temperature profile, as shown in Fig. 3, with the user-defined function. The temperature cycle load is based on Thermotron S-1.2-8200 Benchtop Environmental Chamber, heating from 25° to 110°C in 18 minutes. The period of one cycle of the thermal cyclic test is 72 mins, and the dwell time for the high temperature (383K) and low temperature (233K) is 9 minutes.

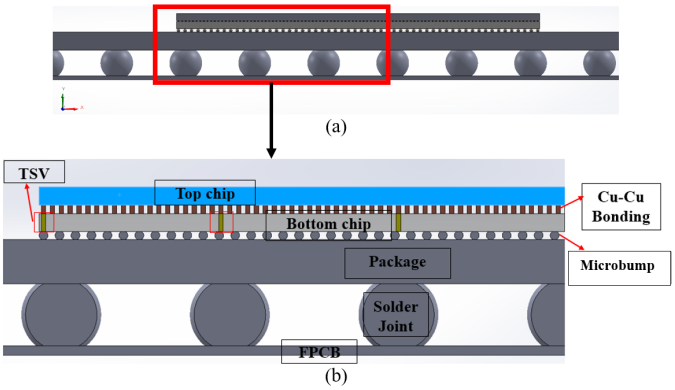

Fig. 1. (a) Front view of the package and (b) Scale-up view of the package

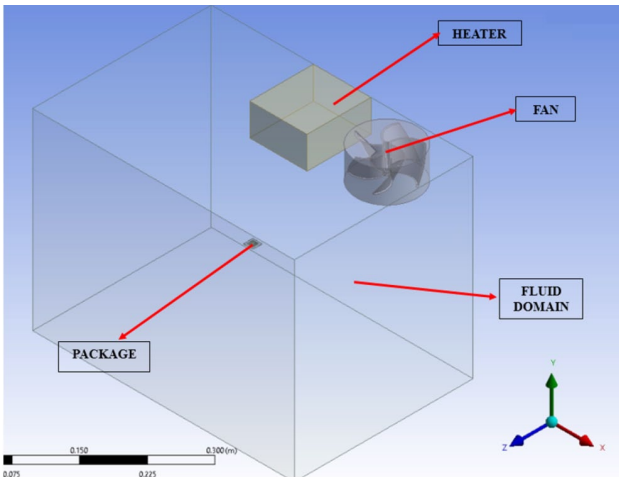

Fig. 2. 3D model of the thermal cyclic chamber

TABLE 1

Dimension and number of parts in a package

Part	Number of Parts	Dimension (mm)
Top Chip	1	5 × 5 × 0.1
Bottom Chip	1	5 × 5 × 0.1
Package substrate	1	9 × 9 × 0.25
FPCB	1	15 × 15 × 0.053
Cu-Cu hybrid bonding	1164	0.025 × Ø 0.025 (spacing 0.05)
Microbump	636	0.045 × Ø 0.05 (spacing 0.09)
TSV	20	0.1 × Ø 0.025
Solder joint	100	0.35 × Ø 0.45 (spacing 0.95)

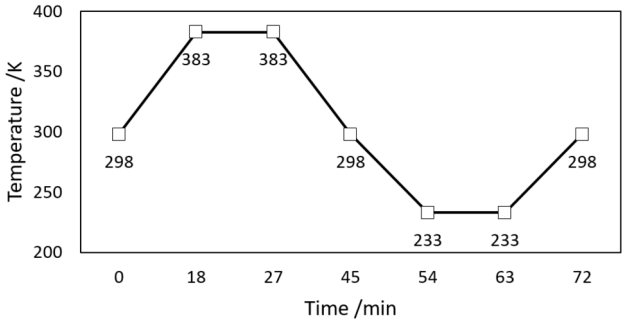

Fig. 3. Temperature Profile of Thermal Cyclic Test

2.3. Grid independence test

Grid independence tests were conducted before the simulation to achieve an optimal mesh density. It is crucial to reduce discretization errors and save computation time for the simulation of the computational domain. Five mesh models of different numbers of elements and nodes were generated for FLUENT and Transient Structural, respectively, as shown in TABLE 2 and TABLE 3. The discretization error was determined by comparing each case to the finest mesh, which is model 5. As the number of elements increased, a decreasing trend in the percentage difference was observed for the tested parameters. Based on the grid independence test, Model 4 was chosen for additional analysis in FLUENT with a discretization error of 0.02%, while Model 3, with a discretization error of 0.33%, was used for Transient Structural due to the optimal in terms of accuracy and computational cost. Khor and Abdullah [16] reported that a 3% or less discrepancy was acceptable for the study.

TABLE 2

Grid independence test for the FLUENT

Model	No of Elements	Temperature (K)	Discretization error
1	592485	379.482	0.83%
2	644907	381.519	0.30%
3	750613	381.060	0.42%
4	890701	382.746	0.02%
5	1579239	382.656	0.00%

TABLE 3

Grid independence test for the Transient Structural

Model	No of Elements	Maximum Thermal Strain	Discretization error
1	152483	0.00280439	6.34%
2	194834	0.00270730	2.66%
3	258857	0.00262850	0.33%
4	323605	0.00265630	0.72%
5	352125	0.00263720	0.00%

2.4. Cu-Cu hybrid bonding height

The parameter used in this simulation is the height of Cu-Cu hybrid bonding, h, which are 0.017 m, 0.019 mm, 0.021 mm, 0.023 mm and 0.025 mm, as shown in Fig. 4. By reducing the height between copper layers in interconnects, the capacitance between these layers can be minimized. The lower capacitance helps in faster signal propagation and reduces power consumption.

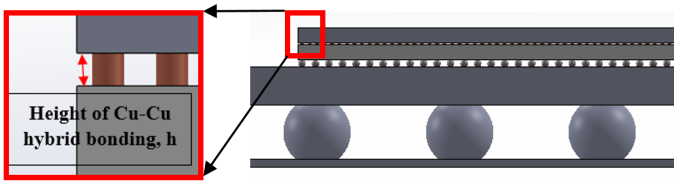

Fig. 4. Scaled-up view of a package with heights of Cu-Cu hybrid bonding

3. Results and discussion

3.1. Model validation

The model validation relies on data from articles and journals as well as a grid independence test to minimize discretization errors. Due to the unavailability of the physical package, the validation process uses these sources to ensure the accuracy of the simulation results. The grid independence test is particularly crucial as it helps confirm that the results are not significantly influenced by the discretization of the computational grid, thereby validating the reliability of the simulation model.

The highest damage was found in two studies by Depiver J. et al. [17,18] like equivalent total strain and equivalent plastic strain are found at the top surfaces of the corner solder joint, which is the same as the current finding. The studies also concluded that the SAC405 solder joint is the most effective under thermal cycling conditions because it exhibits the lowest Von-Mises stress (approximately 200 MPa), which aligns with the simulation results. Specifically, the maximum Von-Mises stress over time for the SAC405 solder joint with a 0.025 mm Cu-Cu hybrid bonding height is 236.75 MPa, while the stress for the other four configurations is around 170 MPa. Another research from Xia Y et al. [19] for the effect of thermal cycling on the strain and stress distribution of TSVs and solder bumps in the stacked package structure under a thermal cycling test between –100°C and 120°C. They found that the second layer has a maximum stress of 345.95 MPa at the temperature of −100°C and a maximum stress of 296.84 MPa at the temperature of 120°C. The maximum stress from the current finding ranges from 392 MPa to 396 MPa within the package.

For the grid independence test in the research of Lee J. et al. [20], Ahmad M. et al. [21] and Ng F. et al. [22], they choose the mesh model with less than 1% of discretization error. Their simulation data has an acceptance range of error of less than 10% compared to the experiment data that validates their model. In this study, the discretization error of the mesh model used in FLUENT is 0.02%, while in Transient Structural, it is 0.33%. Since both discretization errors are less than 1%, the error of simulation data compared to experiment data should be within the acceptance range of less than 10%.This low level of discretization error ensures the accuracy and reliability of the simulation results, making the model robust for predicting the behavior of Cu-Cu hybrid bonding packages under thermal cyclic test.

3.2. Effect on temperature distribution

The temperature of different heights of Cu-Cu hybrid bonding and SAC405 solder joint at 1620s (the end time for the dwell time of high temperature) and at 3780s (the end time for the dwell time of low temperature) have been analyzed. All the temperature distribution and temperature difference dataare tabulated in TABLE 4 and TABLE 5. Based on TABLE 4, the temperature difference of Cu-Cu hybrid bonding with different heights at the 1620s and 3780s is less than 0.1K. It indicates that the temperature across 1164 bodies of Cu-Cu hybrid bonding within the package is almost similar due to their uniform heat transfer. On the other hand, the temperature difference of the SAC405 solder joint with different heights of Cu-Cu hybrid bonding at 1620s and 3780s is more than 1K in TABLE 5. The highest temperature difference is the SAC405 solder joint at 3780s for 0.019 mm height of Cu-Cu hybrid bonding, causing non-uniform expansion. It will lead to stress concentration, especially at the corners and edges of the solder joint.

In Fig. 5, an increasing trend was observed for the maximum temperature at the 1620s, which is the height of Cu-Cu hybrid bonding. This suggests a link between bonding height and the

TABLE 4

Temperature distribution and temperature difference of Cu-Cu hybrid bonding at different heights at the 1620s and 3780s

Height of Cu-Cu hybrid bonding (mm)	Minimum temperature (K)	Maximum temperature (K)	Difference	Minimum temperature (K)	Maximum temperature (K)	Difference
	1620s			3780s		
0.017	382.746	382.746	0	235.512	235.513	0.001
0.019	381.751	381.755	0.004	247.897	247.929	0.032
0.021	382.773	382.773	0	235.680	235.681	0.001
0.023	382.258	382.261	0.003	242.608	242.631	0.023
0.025	382.770	382.770	0	235.836	235.837	0.001

TABLE 5

Temperature distribution and temperature difference of SAC405 solder joint with Cu-Cu hybrid bonding at different heights1620s and 3780s

Height of Cu-Cu hybrid bonding (mm)	Minimum temperature (K)	Maximum temperature (K)	Difference	Minimum temperature (K)	Maximum temperature (K)	Difference
	1620s			3780s		
0.017	382.749	382.762	0.013	235.176	235.427	0.251
0.019	382.291	382.700	0.409	235.773	240.322	4.549
0.021	382.773	382.781	0.008	235.376	235.637	0.261
0.023	382.767	382.974	0.207	235.884	238.517	2.633
0.025	381.442	382.598	1.156	235.379	235.677	0.298

thermal performance of the package. As the height of the Cu-Cu hybrid bonding rises, it may alter thermal conductivity and heat dissipation channels within the 3D package, resulting in greater temperatures. However, a significant anomaly appears, with a sudden decrease in maximum temperature at the 1620s, which was explicitly observed for the 0.019 mm bonding height. This anomaly suggests that more heat energy may be required to raise the temperature of packages with this height compared to others, potentially due to increased thermal resistance or different heat dissipation properties at that specific height.

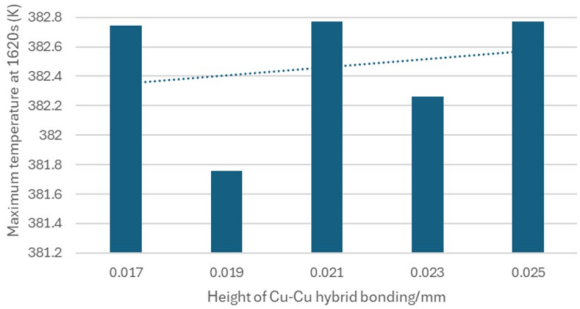

Fig. 5. Maximum temperature at 1620s with different heights of Cu-Cu hybrid bonding

3.3. Effect on thermal strain and Von-mises stress distribution

The decreasing trends in thermal strain and Von-mises stress as the height of Cu-Cu hybrid bonding decreases from 0.025 mm to 0.017 mm are illustrated in Fig. 6 and Fig. 7. The trends observed indicate significant relationships between the heights of Cu-Cu hybrid bonding and various thermal and mechanical responses. When the height of Cu-Cu hybrid bonding decreases, the thermal strain and Von-mises stress at the bonding decrease may be due to several factors. Reducing the bonding height decreases the material for thermal expansion or contraction in response to temperature changes. It will reduce thermal strain as the affected mass decreases. Besides, smaller bonding heights promote uniform stress distribution across the bonded interface while mitigating stress concentrations that can lead to higher Von-mises stress levels in larger bonding.

Additionally, decreased bonding height often correlates with increased mechanical stiffness of the bonded structure, which helps distribute thermal stresses more evenly and reduces the overall magnitude of strain and stress responses. These combined effects contribute to enhanced thermal and mechanical reliability of Cu-Cu hybrid bonding. Based on the research from Sun H. et al. [23] aboutthermal-mechanical reliability analysis of WLP with fine-pitch copper post bumps. They concluded that reducing the height of the copper post from 50 mm to 40 mm leads to a 6.5% increase in solder bumps' average thermal fatigue life. This improvement is attributed to decreased elastic deformation and shear stress within the copper post bumps, enhancing their durability. Research from Lee J. et al. [20]also claimed thatthe maximum deformation of SAC305 solder bumps on Cu pillars shows a decreasing trend as the height of the Cu pillar decreases from 0.15 to 0.09 mm. The 0.017 mm height of Cu-Cu hybrid bonding is the best model due to the lowest thermal strain and Von-mises stress among the five models, as shown in TABLE 6.

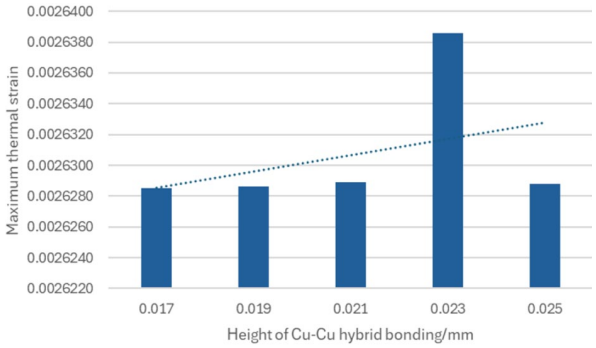

Fig. 6. Maximum thermal strain with different heights of Cu-Cu hybrid bonding

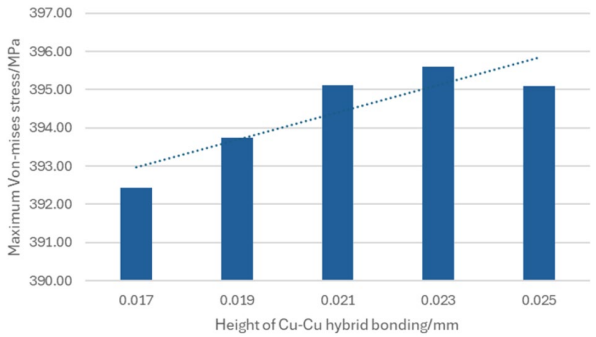

Fig. 7. Maximum Von-mises stress with different heights of Cu-Cu hybrid bonding

TABLE 6

Comparison of maximum thermal strain and Von-Mises stress for different heights of Cu-Cu hybrid bonding

Height of Cu-Cu hybrid bonding (mm)	Maximum thermal strain	Maximum Von-Mises Stress, (MPa)
0.017	**0.0026285**	**392.43**
0.019	0.0026286	393.75
0.021	0.0026289	395.12
0.023	0.0026386	395.60
0.025	0.0026288	395.10

4. Conclusion

This study provides crucial insights into improving the reliability of Cu-Cu hybrid bonding packages. Leveraging thermal-structural simulations explored the thermal and mechanical behavior of 3D stacked die bonding height in minimizing strain and stress. The results validated through literature and grid independence tests confirm that reducing bonding height enhances stress distribution and thermal performance, with 0.017 mm as the optimal height. Decreasing the bonding height reduces the package's thermal strain and Von-Mises stress, thereby mitigating warpage effects. The uniform heat transfer

across different heights of Cu-Cu hybrid bonding and the identified stress concentrations at the solder joint corners align with the findings of previous studies, demonstrating the efficacy of the thermal-structural coupling approach in analyzing these configurations. These findings offer practical guidelines and foundational knowledge for advancing microelectronics design and reliability, supporting engineers and researchers in addressing challenges in packaging technology.

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