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Three-phase voltage outages compensator with cascaded multilevel converter

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Abstract: The paper presents a laboratory prototype of the three-phase transformerless voltage outages compensator with an energy storage based on high voltage supercapacitors. The system described is able to protect an isolated grid e.g. in industry against short voltage interruptions, dips and sags. An idea of a control method as well as a digital controller has been presented, too.

Key words: supercapacitor, voltage dips and sags, multilevel inverter, synchronization

1. Introduction

The public grid is a vast system susceptible to interferences. This forces the need to protect sensitive receivers on the power outage, because even brief interruptions may cause them to malfunction. Traditionally for this purpose one can use uninterruptible power supplies (UPS) equipped in chemical batteries as energy sources. These means allow for maintain power during the interval of several minutes to several hours. In case of short-term voltage disturbances caused by processes such as for instance a short circuit, compensators become an alternative to UPS devices.

A single-phase simplified prototype compensator equipped in a low voltage supercapacitor, was presented in SENE'2007 Proceedings [2]. The paper described the main idea and topology of the line-interactive compensator. A two-level inverter used in the compensator did not minimize a problem of distorted waveforms in generated voltage. Moreover some minor improvements in the synchronization mechanism have been inserted in order to assure a proper sag detection.

The principle of the compensator performance allows to classify it as a special kind of active filtering devices or off-line dynamic voltage restorers (DVR). DVRs that use only supercapacitors (electric double layer capacitors, EDLC) as an energy store do not need any service applied usually to energy storage devices based on batteries. Typically the DVR uses transformers connected in series [10] and injecting relatively high losses to the grid. The

compensator described below is characterized by off-line mode of operation and ability of 100% voltage regeneration regardless of sag depth.

2. Construction of the laboratory model

The novel three-phase compensator laboratory model has been built as a standalone and integrated device and tested in Gdańsk Branch of The Electrotechnical Institute as a result of a special research project COST/255/2006 [1]. The compensator consisted of a three independent one-phase multilevel cascaded inverters and an energy store based on high voltage stacked type EDLCs.

Three identical single phase compensators connected in a star as shown in Figure 1. Each single phase compensator is formed as a cascaded multilevel inverter built from two H- bridges units which are independently supplied. This allows to utilize lower rated voltage of semiconductor switches in order to receive output voltage waveforms of higher amplitudes. Another advantage is concerned to the number of possible voltage steps in the output waveform.

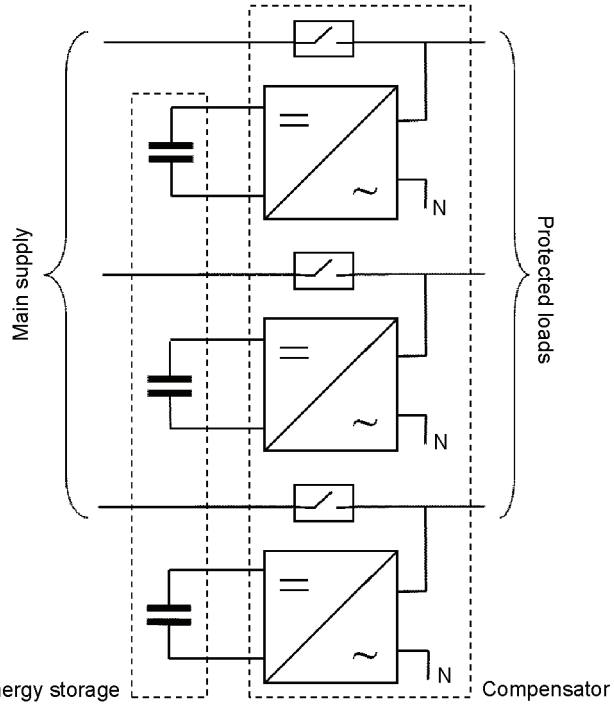

Fig. 1. Block diagram of the three-phase voltage outages compensator

To realize compensation process or active filtering it is possible to use transformerless connection between the compensator device and the voltage power grid [3-5]. Simplified diagram of a single phase circuit is shown in Figure 2.

Energy exchange between the network and the supercapacitor provides the cascade inverter consisting of two H-bridge inverters connected in series and supplied by two DC/DC intermediary circuit converters (P_1 and P_2). The key K denotes a very fast switch placed between phase line and protected network. The switch is able to disconnect the load from the mains. Symbols C and R_L denote parameters of the load. Most of time the switch K is closed allowing energy flow from the mains to load and to the compensator. It must be disconnected at the specific instant of voltage interruption or dip when the compensator takes over to power sensitive loads.

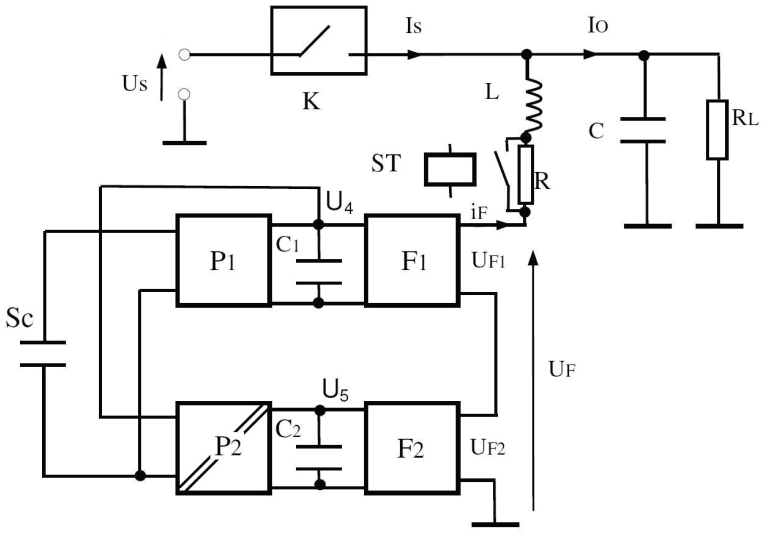

Fig. 2. A simplified diagram of the one phase of the three-phase voltage outages compensator

3. Identification of voltage dips

Fast switching devices or other sudden unexpected disturbances provoke habitually short failures or power outages in the network. The failures may appear at the moment of load on/off switching or as result of short circuits and they are of the stochastic nature. Generally (more than 90%) these failures have a shape of voltage dips or short interruptions. In order to compensate them effectively they must be immediately detected or even anticipated. The rapid diagnostics of the failure state is the elementary condition of the effective compensator performance what makes it possible to "rebuild" the voltage. However methods faster than depicted in [11] were not used because of independent controllers in each phase.

If detection of lower voltage states (dips) occurs when the network voltage and the time base generated by the control circuit are synchronized than it is possible to determine the current voltage amplitude of the first harmonic A_1 of the signal $u_s(t)$. According to the formula (1) the amplitude A_1 is given:

$$A_1 = \left| 2 \cdot \sum_{n=0}^{N-1} u_s(n) \cdot \sin(2\pi n / N) \right|, \tag{1}$$

where: $u_s(n)$ – n-th sample of the input signal, n – input sample index, N – number of input samples or frequency components of the discrete Fourier transform (DFT).

The idea of the actual and reference voltage comparison ("prediction") in an interval T is illustrated in Figure 3. The reference voltage signal is created as a predictive alternating voltage synchronized with the fundamental harmonic of the mains voltage. The comparison process occurs only in selected intervals of the period T. Comparison results during short zero crossing intervals are not taken into consideration. These intervals have been adopted experimentally and set on the value of ± 1.25 ms. Analyzing deviations of the instantaneous voltage outside zero crossing intervals results in that, in the worst case, a delay compensator response to a dip will be in maximum t_{opmax} = 2.5 ms (2 • 0.125 • T/2, T = 20 ms). Nevertheless the likelihood of such events during process comparison is small and the delay will relatively be comparable with the assumed cycle of sampling (e.g. T_p = 80 μs typically). A parameter which better describes the possible delay of dip detections is the expected value. In the presented method this value could be estimated at approximately 0.7 ms as the average delay time course of variability shown in Figure 3b.

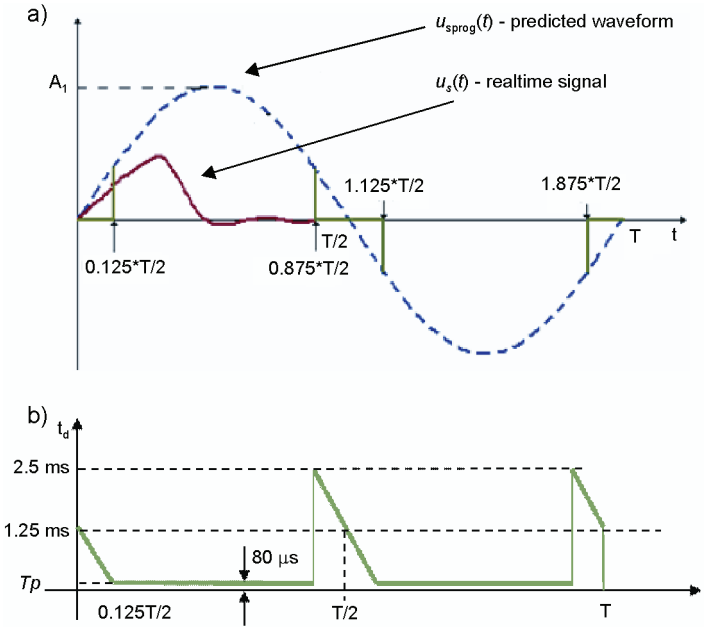

Fig. 3. The detection mechanism: a) comparison of the real and predicted signals in the interval T (one period) and marked zones of measurement insensitivities; b) a way to estimation of average delay of the dip detection

In the case of strong deformation of voltage waveform in the network the above described method may result in detection of dips even though the root-mean-square (rms) voltage is acceptable. In this case the predicted signal should take into account the most likely form of the

forecast. Inclusion of an appropriate reference signal distortion can be obtained taking into account the higher harmonic components. The amplitudes of these components can be calculated using the conversion formula (1).

Effective dips detection, fast and highly immune to noise, requires the use of specialized algorithms, including the synchronization mechanism (described below) by FFT or wavelet transform. The main difference between the wavelet transform described in [8] and DFT is that the first one operates in the time domain while the FFT in the frequency domain and uses variable window sizes to capture voltage changes. But practical implementation to the detection process is still difficult [11].

In [5] the dip detection mechanism was performing in two ways: exploring patterns of instantaneous value deviation and the r-m-s value of the measured waveform.

4. Synchronization with the mains voltage

In order to minimize transients after power outage of the main supply a replacement supply source (loss compensated) must have an amplitude and phase of the voltage compatible with pre-distortion waveform. Compensator controller provides synchronization of the internal reference voltage signal generator with voltage occurring during proper operation of the main power supply by means of phase locked loop (PLL). The applied software method of synchronization with the mains voltage is based on the use of DFT transforms signal $u_s(t)$ into two orthogonal components of the formula:

$$Us(m)\sum_{n=0}^{N-1} u_s(n)\cdot\left[\cos(2\pi nm/N) - j\sin(2\pi nm/N)\right] = \mathrm{Re}\,Us(m) + j\,\mathrm{Im}\,Us(m), \tag{2}$$

where: $Us(m)$ – m-th component of the DFT, m – output component index in frequency domain, $u_s(n)$ – n-th sample of the input signal, n – input sample index, N – number of input samples or frequency components in the DFT.

If the signal $u_s(t)$ is an odd function of time and the period of input signal is $T = T_p \cdot N$ (T_p – sampling period, N – constant) then the real components of DFT will be zeroes:

$$Us(m) = j\sum_{n=0}^{N-1} u_s(n)\cdot\sin(2\pi nm/N). \tag{3}$$

In case of no synchronization, when $T \neq T_p \cdot N$, where T is the period of the signal $u_s(t)$, the real component Re (Us (m)) and imaginary component Im (Us (m)) have nonzero values. The equation (3) describes the synchronization state of the odd components of the signal $u_s(t)$ with the sampling system.

The compensator should synchronize the sampling system with the first harmonic of grid voltage for $m = 1$. The angle between the vector $u_s(1)$ and the real axis is described by the formula:

$$\varphi(1) = \arctan\frac{\mathrm{Im}\,Us(1)}{\mathrm{Re}\,Us(1)}. \tag{4}$$

The synchronization state can be obtained by changing the sampling period T_p in such a way that $(T - T_p \cdot N) \rightarrow 0$. Then the angle defined by formula (4) tends toward $\pi/2$. A simplified angle control system is shown in Figure 4. Only the real component of DFT is calculated and in this way the time-consuming calculation of the function $arctan(\varphi)$ is omitted.

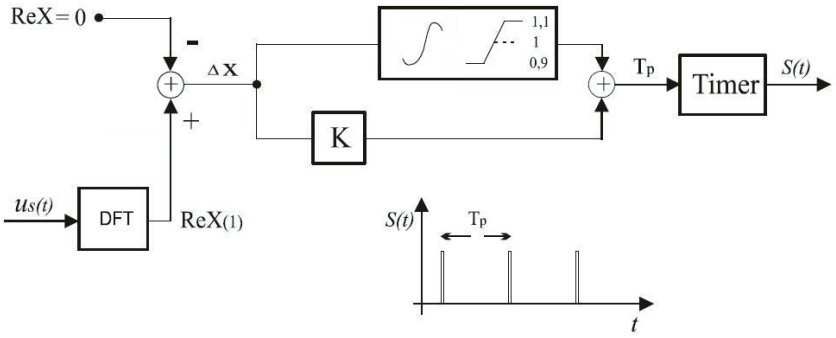

Fig. 4. A simplified synchronization circuit (integration with limitation in the integrating element)

The output signal $S(t)$ is a synchronized time base common to all signal processing blocks in the digital controller, including dependent computational blocks (5) and (6) generating waveforms transistor control described below.

5. Power generation using cascade multilevel inverter

The cascade inverter allows for the generation of stepped output voltage [6-8]. The instantaneous value of the output voltage is $U_F = U_g(nT_p)$. The available voltages based on the DC link voltages U_4 and U_5 of the component inverters shown in Figure 5 are as follows: (U_5), $(U_4 - U_5)$, (U_4), $(U_4 + U_5)$, $(-U_5)$, $(-U_4 + U_5)$, $(-U_4)$, $(-U_4 - U_5)$, 0. The intermediate voltage values (between 0 and $\pm U_5$) are obtained by using pulse width modulation (PWM) according to the formula:

$$Ug(n \cdot T_p) = \begin{cases} U_4 + D \cdot U_5 & \text{for} \quad U_4 < Uz(n \cdot T_p) \\ U_4 - D \cdot U_5 & \text{for} \quad (U_4 - U_5) < Uz(n \cdot T_p) < U_4 \\ D \cdot U_4 + (1 - 2 \cdot D) \cdot U_5 & \text{for} \quad U_5 < Uz(n \cdot T_p) < U_4 - U_5 \\ U_5 \cdot D & \text{for} \quad 0 < Uz(n \cdot T_p) < U_5 \\ -U_5 \cdot D & \text{for} \quad 0 > Uz(n \cdot T_p) > -U_5 \\ -D \cdot U_4 - (1 - 2 \cdot D) \cdot U_5 & \text{for} \quad -U_5 > Uz(n \cdot T_p) > (-U_4 + U_5) \\ -U_4 + D \cdot U_5 & \text{for} \quad (-U_4 + U_5) > Uz(n \cdot T_p) > -U_4 \\ -U_4 - D \cdot U_5 & \text{for} \quad -U_4 > Uz(n \cdot T_p) \end{cases} \tag{5}$$

where: $n = 0, 1, ..., 255$.

The value D represents the ratio between the transistor switch-on time ΔT and the current value of the sampling period T_p. During the dip occurrence the compensator should generate the desired voltage with amplitude and frequency according to the following equation:

$$Uz = A_{1z} \cdot \sin\left(2 \cdot \pi \cdot \frac{n \cdot T_p}{T}\right), \tag{6}$$

where: A_{1z} – required first harmonic amplitude, T – grid voltage period.

The calculation of the parameter D for each n, necessary to determine the instantaneous values of voltage Uz is done by comparing right sides of formulas (5) and (6). The authors of work [9], analyzing the symmetrical three-phase cascade inverter (with equal voltage sharing in DC link circuits and without auxiliary DC converters as in the presented construction), pointed out the possibility of lowering the carrier frequency in proportion to the number of component inverters by using an unipolar sine-wave PWM modulation with a phase shift.

6. The voltage balance of the cascade converters

The simplified structure of one phase compensator is shown in Figure 2. For the asymmetrical cascade solution it has been assumed that the ratio of converters DC link voltages is:

$$U_4/U_5 = 3. \tag{7}$$

This expression is derived directly from the principle of creating the stepped waveform in multilevel inverter with uniform gradation of the output voltage [1, 7]. This voltage balance for capacitors C_1 and C_2 is held in every working state by P_2 converter (Fig. 2) approximating an idea depicted in [12]. When converters P_1 and P_2 are disconnected the balance between the voltages U_4 and U_5 is determined by the ratio of time constants of intermediate circuits R_1C_1 and R_2C_2.

Considering the condition (7) the calculation implementation in the microcontroller provides for inverters switching with carrier frequency ensuring the short-term output voltage U_F amplitude changes not exceeding $2 \cdot U_5$. This limits the voltage stress for cascade inverter output semiconductors and determines the dimensions of the filter. Additionally, in standby state, while waiting for the voltage disturbance, the condition $U_5 + U_4 > A_1$ should be executed, to assure the appropriate relationship between the grid voltage amplitude A_{1z} and the intermediate circuit voltage calculated according to equation (1). To achieve this the voltage U_5 is regulated using the inverter's $F2$ zero vector and isolated converter P_2. In Figure 5 an example of current flow path during charging for positive polarization of the grid voltage is presented.

7. The laboratory model construction

The compensator consists of three identical converters. Each converter is connected in parallel to the appropriate phase of the protected network and operates independently. The

balance of currents in the point of common coupling of the network, load and compensator is as follows:

$$I_S + i_F = I_O. \tag{8}$$

The main energy storage in each phase is accomplished by high voltage supercapacitor Sc 2 F / 300 V, manufactured by ECOND. The energy storage capacity of this component is approximately 90 kJ.

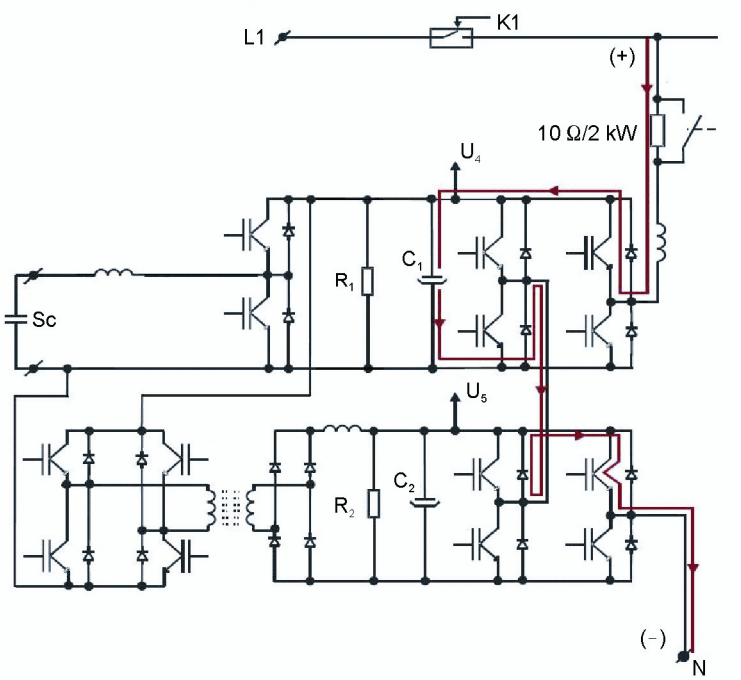

Fig. 5. Schematic diagram of one phase of the compensator. The half-wave alternating current path during pre-charge of the capacitor C_1 is marked

The adopted compensator topology requires the usage of mutually isolated power converters (blocks P1 and P2) and inverter bridges F1 and F2 forming the asymmetrical multilevel inverter operating as inverter or rectifier charging the supercapacitor Sc energy storage. The converters have been realized using electro insulated IGBT modules IPM 200 A/1200 V manufactured by Mitsubishi. The single module contains two power switching elements with power diodes and gate circuits. For the cores of inductive components i.e. transformers and reactors the amorphous magnetic material with high saturation induction (type 2605SA1, Metglas) in the form of a slot-shaped CC has been chosen. As an AC switch K the thyristor electroinsulated module with rated current 125 A (Crydom) has been used. The converters F1 and F2 are connected to the grid through LC filter circuit and the resistor for pre-charging electrolytic capacitors C_1 and C_2 to establish intermediate constant voltages of U_4 and U_5, which can be bypassed by the switch.

In the control part of the compensator an integrated controller card with a CPU unit based on a signal processor TMS320F2812 (Texas Instruments) is used. The controller is coupled with the transistor modules using fiber-optic cables. Due to the short operating time and in accordance to this, semi-adiabatic power components cooling processes, the elaborate cooling system for heat transfer from the semiconductor switches was not necessary.

The three-phase energy storage facility is shown in Figure 6b. It has been located in separate compartment and connected to the compensator by the cable line.

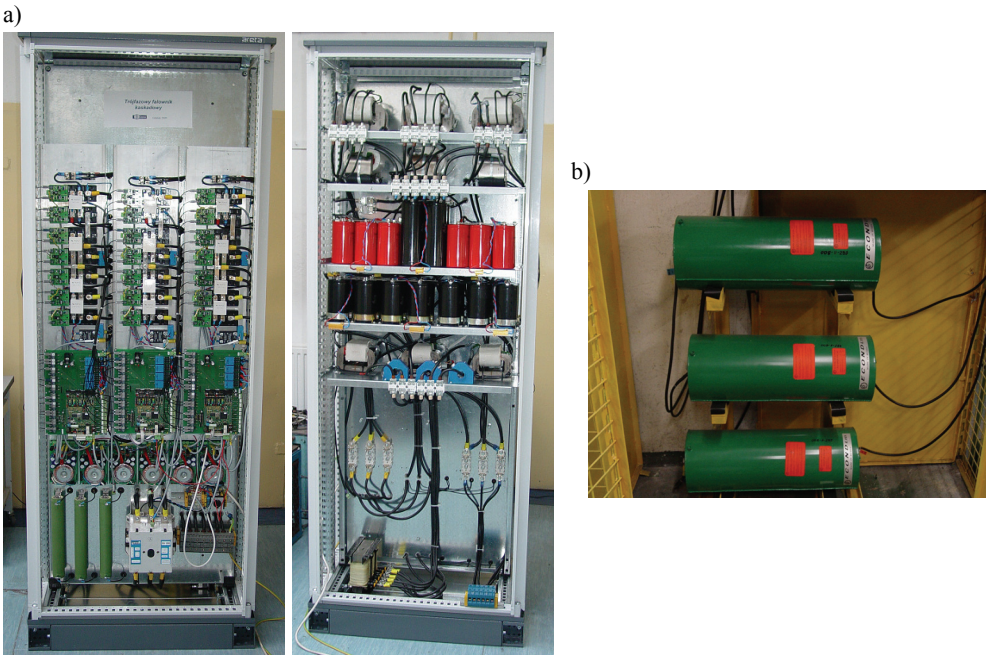

Fig. 6. A view of the tree-phase compensator construction: a) front and rear rack carrier, b) supercapacitors

8. Description of the compensator algorithm

The operation of the compensator requires realization of multiple concurrent real-time control tasks. In order to solve the complexity of these issues the finite-state machine (called a finite automaton) has been created in the controller of the compensator. Six basic states of operation have been distinguished in the control algorithm:

STOP off – no mains power.

CHARGE C2 device is powered and supply voltage (*Us*) is normal. Capacitor C_2 is charged to the voltage $U_5 = 0.33A_1$, where A_1 is the first harmonic amplitude of the mains voltage.

CHARGE C1 device is powered and supply voltage (*Us*) is normal. Capacitor C_1 is charged to the voltage $U_4 = 0.8A_1$

WAIT standby – waiting for dip or voltage outage

CHARGE Sc charging the supercapacitor *Sc* in given compensator's phase. The charger raises and maintains the level of the supercapacitor voltage at $U_{sc} = U_{p2} =$ = 300 V.

INVERTER based on the energy stored in supercapacitor *Sc* phase voltage is generated using the cascade inverter. The device enters this state after the identification of voltage dip or power failure.

Figure 7 shows the simplified operating graph for the created finite-state machine with the conditions for transitions between states. These conditions are discrete variables (logical states 0 or 1), obtained by simple comparisons or as the result of more complex calculations (dip detection – SAG_DET). Threshold values U_{P1} and U_{P2} determine supercapacitor working voltage range.

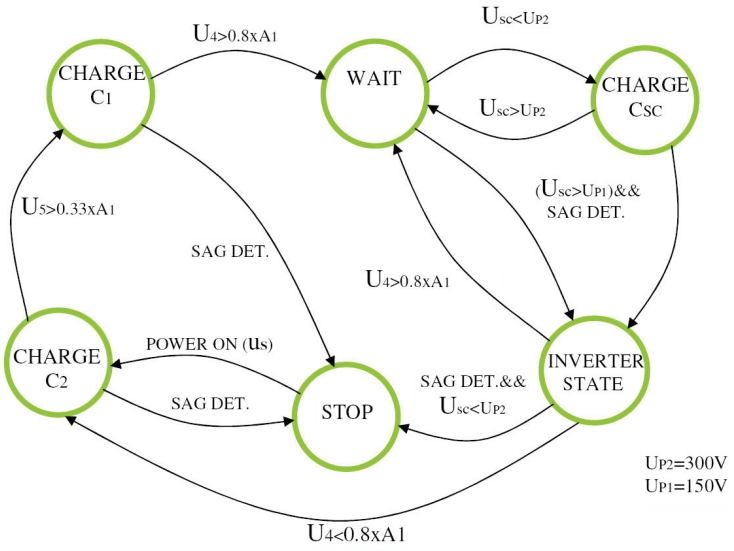

Fig. 7. A simplified graph of the operating states of the voltage compensator

In addition to the grid voltage measurement, waveforms synchronization, compensating voltage generation and regulation of energy flows between the grid, energy storage and load, the controller also supports communication with higher level control system using local or wide area network.

8. Experimental results

The oscillogram presented in Figure 8 illustrates the PWM operation together with a stepped modulation, which form the output voltage waveform of the compensator.

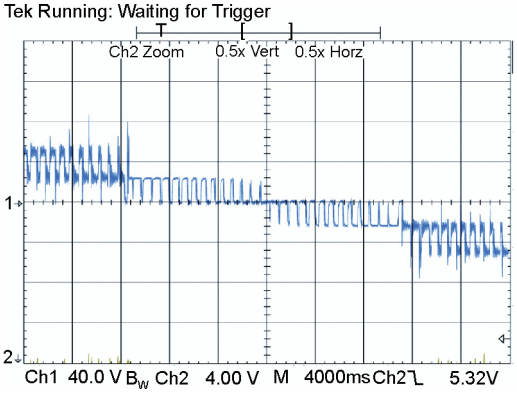

Fig. 8. The magnified view of the output waveform of the cascade inverter showing voltage modulation

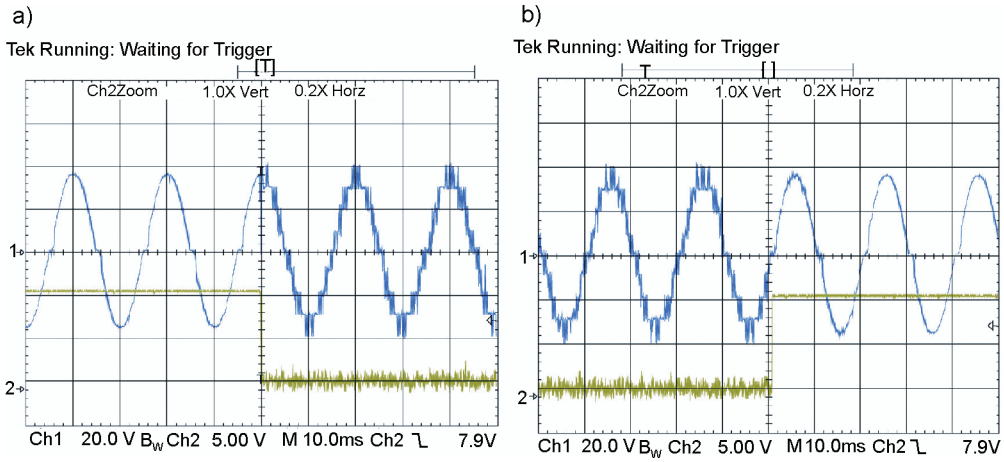

Fig. 9. Laboratory test waveforms showing the start (a) and the end (b) of the voltage generation by the cascade inverter

Figure 9 shows the voltage waveforms illustrating the operation of the compensator in response to grid voltage disturbances. The fast switching from network to supercapacitor storage supply is shown in Figure 9a and back switching after restoring the network voltage is shown in Figure 9b. The slight deformation of the obtained voltage around zero crossing points is caused by the properties of thyristor switch K at low voltage.

10. Conclusions

A great and still escalating number of non-linear loads and growing share of energy from distributed resources result in decreasing the reliability of the public power grids. Therefore the issues related to the improvement of the quality and reliability of the electrical energy supply are particularly important.

The presented compensator model allows for compensating dips and short-term interruptions in a three-phase four-wire grid. The device consists of three one phase cascade multilevel voltage converters. The high voltage stacked supercapacitors are used as energy storage for the compensator. The usage of such an energy storage devices has many advantages, but till now is not practically implemented in energetic supply systems, mainly because this technology is not widely known yet and high voltage supercapacitors are still very expensive.

The observed rapid progress in supercapacitors' technology will undoubtedly lead to mass production of these components with better parameters and much lower price, which will allow the wide usage of supercapacitor based compensators for protection of the sensitive processes and devices against interruptions or voltage dips in supply networks or for suppressing disturbances in networks with disruptive sources.

Acknowledgement

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