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64 Channel ASIC for Neurobiology Experiments

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***Abstract*—This paper presents the design and measurements of 64 channel Application Specific Integrated Circuits (ASIC) for recording signals in neurobiology experiments. The ASIC is designed in 180 nm technology and operates with ± 0.9 V supply voltage. Single readout channel is built of AC coupling circuit at the input and two amplifier stages. In order to reduce the number of output lines, the 64 analogue signals from readout channels are multiplexed to a single output by an analogue multiplexer. The gain of the single channel can be set either to 350 V/V or 700 V/V. The low and the high cut-off frequencies can be tuned in 9 ÷ 90 Hz and in the 1.6 ÷ 24 kHz range respectively. The input referred noise is 7 μV rms in the bandwidth 90 Hz - 1.6 kHz and 9 μV rms in the bandwidth 9 Hz - 24 kHz. The single channel consumes 200 μW of power and this together with other parameters make the chip suitable for recording neurobiology signals.**

***Keywords*—Low noise amplifier, neural recording, ASIC, multichannel systems, neurobiology experiments.**

I. Introduction

ACCESSIBILITY of modern semiconductor technologies makes it possible to produce electronic multichannel systems consuming low power and occupying small area. Also biotechnology has made a large progress and offers biocompatible multichannel electrodes for neurobiology experiments. Thus in the last decade there is a rapid growth of projects [1] which aim to build measurement systems able to record neurobiological signals from many neurons at the same time. All of these researches are conducted since people like to delve into nervous system in order to understand how it works. This knowledge can be then very helpful in building artificial prosthesis for disabled persons, in finding cures for diseases such as Parkinson or Alzheimer or in reusing it for coding the large amount of information [2], [3].

The main obstacle with such applications is a need to collect the information from many (hundreds or even more) neurons simultaneously what leads to multichannel architectures of recording system. Thus one has to consider an application containing dozens of identical recording channels which main requirements are:
- low power consumption of the single channel (less than 500 μW) in order to preserve the tested tissue from overheating [4] and also to ensure long term recording in the case of using battery power supply,
- small area occupied by the entire electronic chip in order to build light recording system essential for in vivo experiments,
- good uniformity of the main chip parameters such as corner frequencies of the recording channel, its gain and input referred noise,
- low input referred noise in order to record small input signals which amplitudes are from tens to hundreds of μV,
- good functionality (the ideal would be the system able to record various neurobiology signals [5], so the one with possibility of changing its frequency band and gain, both in the wide range).

Despite all above requirements one has also to take into account other aspects of such systems. For instance, recording signals situated in a single Hz frequency band forces consideration of flicker noise 1/f component which in modern VLSI technologies dominates in this frequency range. One has also to take into account large DC voltage offset which is generated at the electrode-tissue interface and can be large enough to saturate the input stage of recording amplifier. Additionally, the need of recording signals with very low frequencies (even below 1 Hz) obligates a designer to use filters with very large RC constants. This means that one has to employ high resistance structures which in modern technologies with limited silicon area is difficult to obtain.

The mentioned restrictions are sometimes mutually opposing (e.g. low input referred noise and low power consumption or good uniformity of the main parameters and small area occupied by the designed chip) which complicates a final chip and forces one to find optimized solutions.

Based on our experience in design and practical applications of such kind of ASICs for recording systems comprising of hundreds of electrodes [6], [7], [8] we propose a new 64-channel ASIC, which meets the above requirements.

The paper is organized as follows. Section II describes the ASIC architecture. The measurements are presented in the Section III and Section IV contains conclusions.

II. Chip Architecture

In the Fig. 1 the microphotograph of the chip is presented with main blocks described. The Fig. 2 illustrates the architecture of a single recording channel. It consists of two amplifying stages AMP1 and AMP2 and an analogue multiplexer.

The input capacitor C_1 separates the amplifier from the large DC offset generated on the electrode-tissue interface. The feedback of the front end amplifier is based on the C_2

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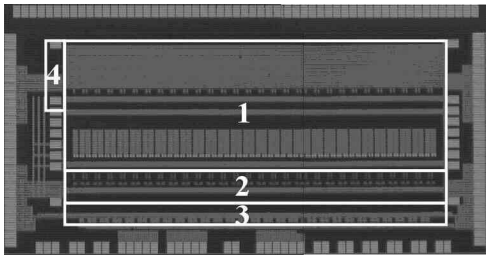


Fig. 1. Photo of the 64-channel chip where: 1 - AMP1, 2 - AMP2, 3 - analogue multiplexer, 4 - voltage references.

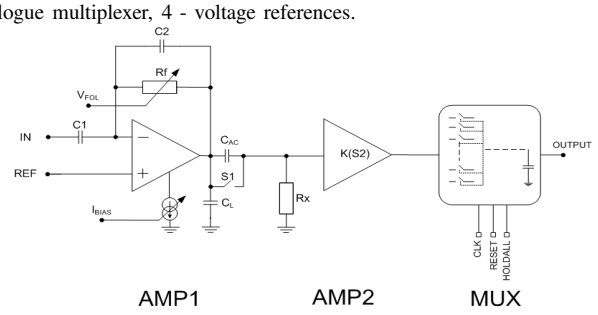


Fig. 2. Simplified block diagram of single readout channel.

capacitor and the active R_f resistive block. The R_f resistance is responsible for biasing the input of the differential amplifier and for setting the low cut-off frequency. These elements are responsible for setting the voltage gain and low cut-off frequency according to the equations:

$$K_V \approx -\frac{C_1}{C_2} \tag{1}$$

$$f_d \approx \frac{1}{2\pi R_f C_2} \tag{2}$$

The overall input referred noise of the first amplifying stage depends on the operational amplifier noise and its feedback capacitances according to the relation [9]:

$$\overline{v_{ni,amp}^2} = (\frac{C_1 + C_2 + C_{in}}{C_1})^2 \overline{v_{ni}^2} \tag{3}$$

where C_{in} is an input capacitance of the operational amplifier and v_{ni} is an input referred noise of the operational amplifier.

To obtain high voltage gain, low cut-off frequency and to not multiply AMP1 input referred noise, value of the C_1 capacitor is set to the 165 pF while the C_2 is set to the 500 fF. Since input signals are on the level of μV and in order to save a silicon area the C_1 is built using the MOS transistor (W_{MC1}/L_{MC1}= 400 μm/50 μm) working in the strong inversion region. Shifting this transistor into the strong inversion region makes the effective area of C_1 capacitor six times smaller comparing to its counterpart based on the MIM (metal-insulator-metal) capacitor available in the used 180 nm technology. Since the output signals of the AMP1 stage have amplitudes of a few hundred of mV using the C_2 capacitor as a MOS transistor is inadvisable because these signals may modulate MOS capacitance and thus introduce signal distortions. For this reason C_2 is based on the MIM capacitor. The R_f resistance is built as the array of eight PMOS transistors with W_{Rf}/L_{Rf} = 0.5μm/25μm each. User has a possibility to change its resistances by an external input and thus to control the low cut-off frequency. In order to change the high cut-off frequency of the recording channel the external input I_{BIAS} controlling the biasing current of the AMP1 is given.

Preamplifier AMP1 is followed by a second stage amplifier AMP2 which adds additional gain and separates the noisy multiplexer from the sensitive output of the front end amplifier. User has a possibility to change its gain by an external switch S2 either to 1 V/V or 2 V/V. In order to check how DC coupling influences the parameters of the channel we used additional MOS transistor based switch S1 to change amplifiers coupling. The final part of the channel is a 64 : 1 analogue multiplexer which works nominal with 2.5 MHz frequency clock. This results in the 30 kHz sampling frequency per one channel. The multiplexer has an additional functionality, which allows to test only one selected channel [10].

A. *Front End Amplifier*

The front end amplifier is based on the two transconductance amplifiers based on M1 ÷ M8 transitors schematically presented in the Fig. 3.

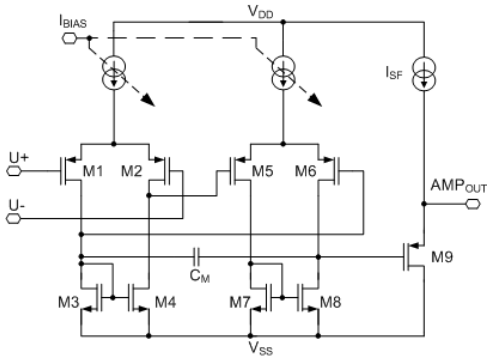


Fig. 3. Simplified scheme of the AMP1.

In order to decrease the influence of the 1/f noise the transistors in the input pair have large dimensions of W_1/L_1= W_2/L_2=700μm/0.5μm and are sourced by the 2.8 μA current each. Open loop gain of this amplifier is 75 dB and the bandwidth limited by the MIM capacitor C_M (equal to 10 pF) is 200 Hz. In order to tune the high cut-off frequency of the amplifier the I_{BIAS} input, controlling the currents sourcing the differential amplifiers, is given.

The critical point of this stage is its feedback circuit. A popular solution [4], [11] employed for building a high value resistances is a MOS bulk diode forming the MOS-bipolar

transistor. It allows to obtain very high resistances up to even 10 TΩ [12] which leads to very low cut-off frequency necessary in the Local Field Potential (LFP signals) measurements. The main disadvantages of such solutions are a strong dependence of the resistance value on the technology in which it was processed, limited control of such a resistance and large resistance spread from channel-to-channel which makes it difficult to obtain acceptable matching of the low cut-off frequencies in multichannel ASIC.

For this reason we used another solution, where a feedback resistance responsible for both setting the low cut-off frequency and biasing the input differential amplifier transistor is user dependend (see Fig. 2). The R_f resistance is built with the PMOS transistors combined as it is shown in the Fig. 4. Gate potentials of the feedback transistors MR1, MR2 are referenced either to the input or output of the AMP1 by the Level Shifters (LS). In order to control resistance of the MR1, MR2 transistors the V_{FOL} input is given. For the test purposes the I_{POL} input is provided to investigate the influence of the bulk polarization on the feedback MOS resistance. Both of them (V_{FOL}, I_{POL}) change the voltage shifting level of the LS circuits. The LS circuits are simple source followers with controlled gate-source voltage by the means of its current.

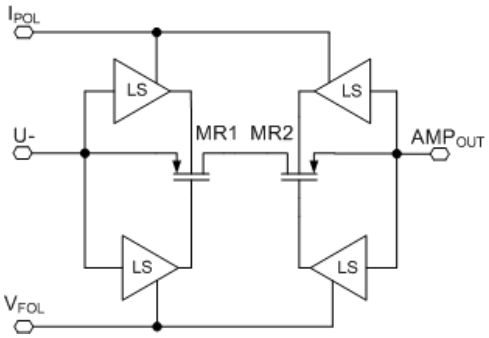


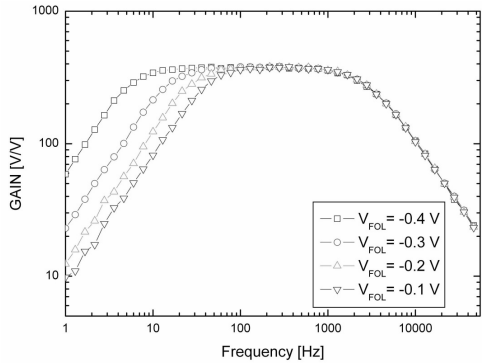
Fig. 4. Simplified scheme of the AMP1 resistive feedback.

III. Measurement Results

In order to perform tests of the described chip the 6 layer PCB board was designed equipped with the LVDS transmitters dedicated for chip communication. All measurements were performed using the NI-6259 measurement card and Lab-VIEW environment. Measurement results of the designed chip are presented below.

A. Pass-Band Settings

In the Fig. 5 the frequency responses for different channel settings are shown. Low cut-off frequency may be changed from 9 Hz up to 90 Hz thanks to the V_{FOL} input controlling the resistance of the AMP1 feedback. Next by changing the I_{BIAS} input in the range 0.1 V ÷ 0.4 V the high cut-off frequency may be set in the 1.6 kHz ÷ 24 kHz range.



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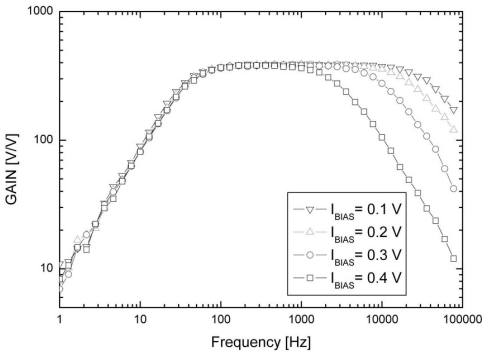


b)

Fig. 5. Frequency response of single channel: a) low cut-off frequency tuning, b) high cut-off frequency tunning.

B. Channel-To-Channel Uniformity

In multichannel chip uniformity of analogue parameters from channel-to-channel (i.e. gain, cut-off frequencies) is the crucial aspect. In Fig. 6, 7, 8 the measured spread of a gain and cut-off frequencies are shown. These demonstrate that the spread of the gain is about 2 % while the spread of the low and high cut-off frequencies are 10 % and 4.5 % respectively. The spread of the low cut-off frequency (which is higher than the other parameters) depends on the feedback capacitance and the effective feedback resistance. The effective feedback resistance is controlled by the level shifters which makes the overall spread of low cut-off frequency higher comparing to solution without such a control [13].

The Table I presents the spread of low cut-off frequency for different corner frequency settings. The spread decreases with increasing corner frequency, however in all cases it is within acceptable limit. Nevertheless this point of design is going to be improved in further version of this chip by using correction DAC's situated in the each recording channel independently.

TABLE I
Spread of Low Cut-Off Frequency vs. Its Mean Value Setting

Low cut-off frequency [Hz]	Spread of the low cut-off frequency [%]
9	22
20	16
36	10

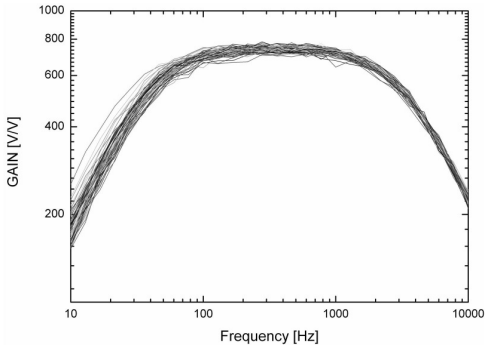


Fig. 6. Distribution of the gain for V_{FOL}= -0.2V.

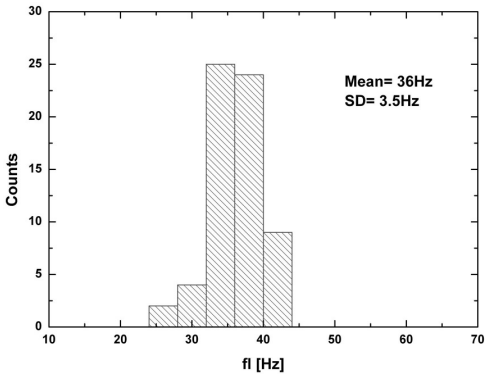


Fig. 7. Distribution of the low cut-off frequency for V_{FOL}= -0.2V.

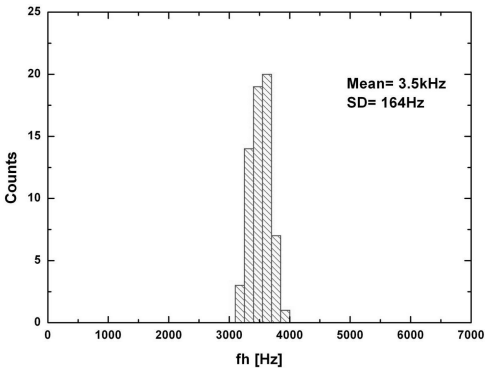


Fig. 8. Distribution of the high cut-off frequency for V_{FOL}= -0.2V.

C. Noise Measurements

The Input Referred Noise (IRN) measurements were also taken. In order to show how the frequency band may influence the IRN the two opposing settings of the channel frequency band were employed:
- Seeting I - frequency band: 9 Hz ÷ 24 kHz,
- Seeting II - frequency band: 90 Hz ÷ 1.6 kHz.

Power spectral density measurements (see Fig. 9) show the frequency band impact on the overall channel noise. Also recorded channel output signals (see Fig. 10) show this relations.

Noise measurements show that for Setting I and Setting II input referred noise are equal 9 μV and 7 μV respectively which are low enough for most in vivo and experiments.

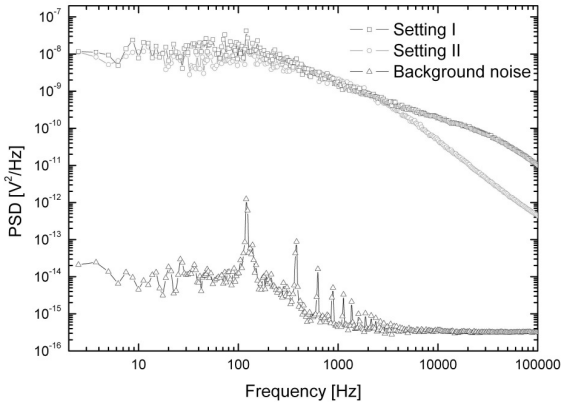
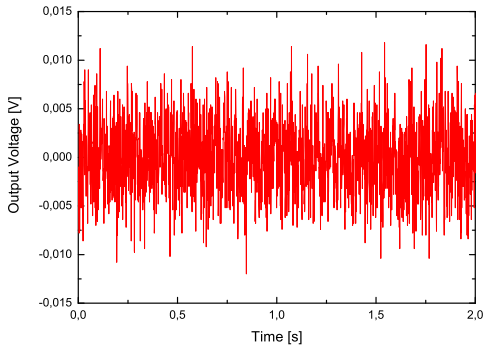
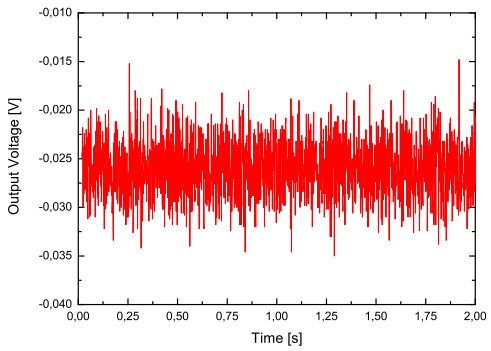


Fig. 9. Power spectral density of output noise of ASIC for two different pass-band settings and instrumentation noise.



a)



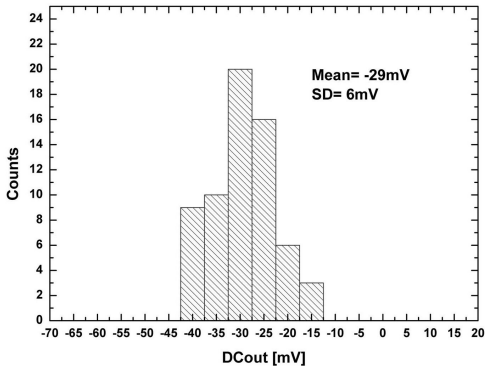
b)

Fig. 10. Typical output reffered noise of the channel for diffrent pass-band settings: a) Setting I, b) Setting II.

D. DC Coupling of the Consecutive Stages

So as to avoid propagation throughout the recording channel of the AMP1 DC offset the C_{AC} coupling capacitor

is used between AMP1 and AMP2 stages (see Fig. 2). The drawback of this solution is that it occupies additional area of the ASIC and introduces a very large time constants in the readout channel (because its corner frequency must be set to not suppress signals from single Hz band). These large time constants are crucial when the system is equipped with the stimulation circuits because the stimulation pulses may saturate input stages of the recording preamplifiers. As a result saturation of the AMP1 stage combined with the AC coupling circuits can increase the time between recording and stimulation phases. Thus we checked the DC spread of the channel output voltage with and without the AC coupling between the amplifying stages. The results (see Fig. 11) show that the channel work with the DC coupling is possible and its DC level spread is still acceptable by an external ADC converter.



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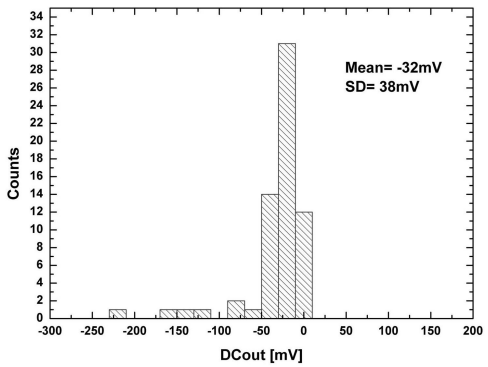

b)

Fig. 11. Distribution of the output DC voltage for internal AC coupling: a) switched on, and b) switched off.

Nevertheless DC coupling of the recording channel may be limiting factor in systems where high channel gain is desirable. Thus we also checked whether it is possible to obtain high voltage gain of the recording channel while the DC coupling of the following stages is set. The Fig. 12 confirms that our 64 channels ASIC are capable to work properly with the DC coupling between amplifier stages and the channel-to-channel uniformity is preserved even in the case of the high gain setting.

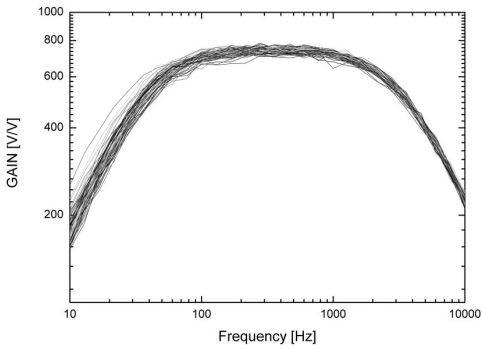

Fig. 12. Frequency response of the 64 channels for 700 V/V voltage gain with the DC coupling set.

E. Systems with Multi-Electrode Arrays

We made an experiment using our prototype board and Multi-Electrode Array (MEA) provided by the Ayanda Biosystems. Into the saline solution in which MEA electrodes were immersed we dipped a metal round electrode with the signal conveyed from the generator. The recorded signals are depicted in the Fig. 13.

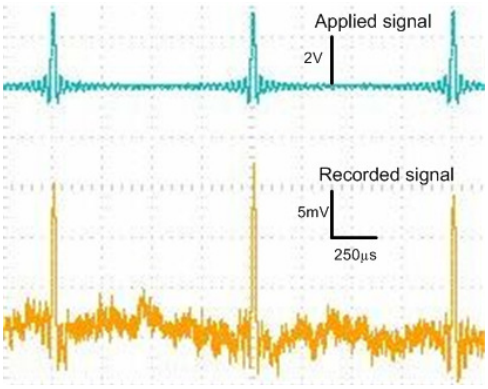

Fig. 13. Signals recorded with the MEA usage.

We have also designed a system for in vivo neurobiology experiments (see Fig. 14) which consists of the presented ASIC and 64 channel electrodes provided by the NEURONEXUS. Data acquisition will be made thanks to the PXI module (PCI eXtension for Instrumentation from National Instruments) equipped with the NI-PXI 6733 card and 100 MS/s, and 14-Bit Digitizer NI-PXI 5122. Overall system is controlled by the LabVIEW made application and will be used for measuring neural signals from the rat under anesthetic. We are going to start the neurobiology experiments soon.

IV. Summary

We presented the design and measurements of the 64 channel chip dedicated for neurobiology experiments. The

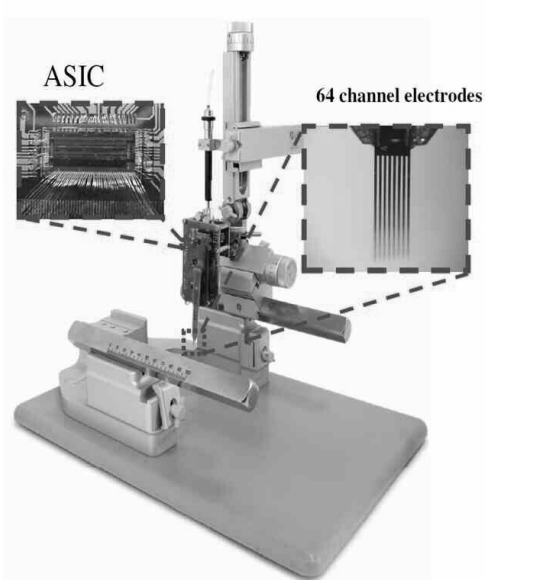

Fig. 14. 64 channel system for in vivo experiments.

ASIC is processed in 180 nm technology and its total area is about 13 mm^2. Its essential parameters are summarized in Table II. The spread of the analogue parameters of the chip makes it suitable for building multichannel measurement system. The system has ability to control its gain and the cut-off frequencies which makes it useful to adapt into different neurobiology experiments.

TABLE II
SUMMARY OF BASIC PARAMETERS OF ASIC

Parameter	Value
Gain	700 / 350 V/V
Tuning range for low cut-off frequency	9 ÷ 90 Hz
Tuning range for high cut-off frequency	1.6 ÷ 24 kHz
Equivalent input noise (depends on bandwidth setting)	7 ÷ 9 μV
Power per channel	200 μW
Power supply voltage	± 0.9 V

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