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ANALOGUE CMOS ASICs IN IMAGE PROCESSING SYSTEMS

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Abstract

In this paper a survey of analog application specific integrated circuits (ASICs) for low-level image processing, called vision chips, is presented. Due to the specific requirements, the vision chips are designed using different architectures best suited to their functions. The main types of the vision chip architectures and their properties are presented and characterized on selected examples of prototype integrated circuits (ICs) fabricated in complementary metal oxide semiconductor (CMOS) technologies. While discussing the vision chip realizations the importance of low-cost, low-power solutions is highlighted, which are increasingly being used in intelligent consumer equipment. Thanks to the great development of the automated design environments and fabrication methods, new, so far unknown applications of the vision chips become possible, as for example disposable endoscopy capsules for photographing the human gastrointestinal tract for the purposes of medical diagnosis.

Keywords: analog CMOS circuits, early vision processing, switched current filters.

1. Introduction

The charge coupled device (CCD) technique has been used for several decades for image sensors due to its high sensitivity, low level of fixed pattern noise (FPN), small dimensions of a photo sensitive device, and the possibility of designing high-resolution matrices. This technique, despite its many advantages, is not optimal for low-cost, low-power image sensors that require integration of a photo-sensitive matrix and a sub-system for vision processing on the same silicon substrate. For this reason, in the last decade a complementary metal oxide semiconductor (CMOS) technology has increasing interest [1-2]. Using CMOS technology it is possible to design a highly integrated complete vision system on a chip (SoC), which is very convenient for high volume production, allowing a significant reduction of unit costs. On the other hand, the photo sensors designed in CMOS technology have worse performance, in particular as regards the image contrast and noise. As the result, a typical CMOS photo-sensitive matrix generates a low quality image, which needs additional low-level pre processing to match the quality of images produced by the CCD sensors. Therefore, the CMOS photo matrices are always designed with the accompanying processors responsible for image enhancement. The general idea of image processing in so-called vision-chips integrated using CMOS technology is explained in Fig. 1. The possibility of producing low-cost vision systems is of particular importance in robotics, intelligent vehicles, or other equipment with small autonomous power sources, as for example disposable endoscopy capsules for photographing the human gastrointestinal tract for the purposes of medical diagnosis [3-5]. In such applications, it is essential to obtain a high speed of image processing with the possibility of extracting high-level information at a very reduced power consumption.

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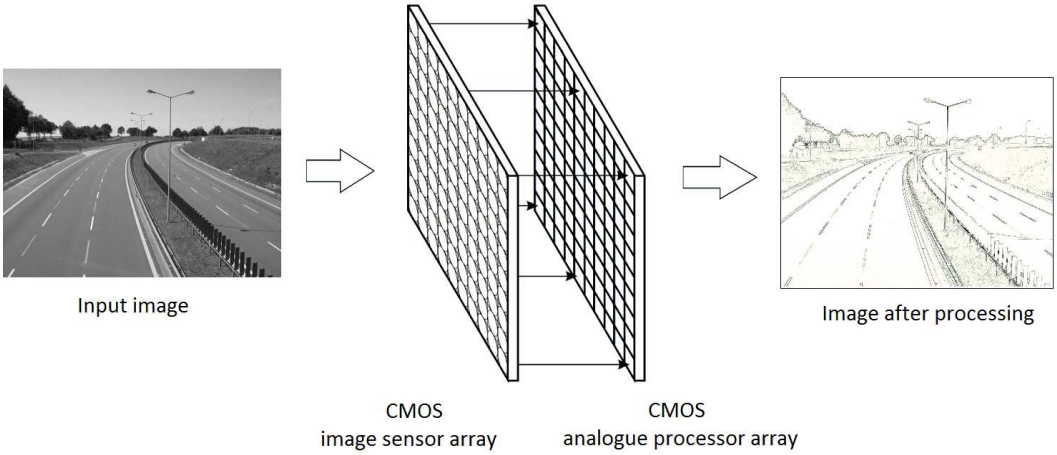

Fig. 1. Image processing stages in a vision-chip.

There are two main types of the vision chips, using analog and digital signal processing. The digital vision chips offer more precise image processing, but consume more supply power at the same processing speed, and require a greater chip area for implementation. The analog versions are more advantageous in this respect, but have limited accuracy. However, in many automation systems their limited accuracy is quite sufficient. In such applications, particularly preferred are the discrete-time analog processors with switched current (SI), due to their compatibility with the standard CMOS technology. This kind of circuits allow achieving a good compromise between complexity and accuracy of signal processing. Intensive research on specialized high-speed analog vision chips with reduced supply power is observed. Confirmation of this fact can be found in the literature, where the analog vision chips [6-16] are faster and consume less power than the digital realizations [17-18]. The remainder of this paper is devoted to a general discussion, in Sec. 2, on the main types of vision chip architectures and their properties. The next section presents a detailed description of a set of high-performance filters, that illustrates the application of the SI technique to image processing. The last section presents the final discussion and conclusions.

2. Architectures of the vision chips

2.1. Typical operations carried out on images

The choice of a vision system architecture depends on the type of operations performed on the image [19]. The operations performed on two-dimensional images can be classified in terms of the amount of data and how it is transferred to the analog processors, as Fig. 2 explains.

The pixel-wise operations require only the value of a currently processed pixel, and no information from neighboring pixels is needed. The following operations: offset, contrast, and gain correction (i.e. histogram manipulation), thresholding, logic operations on binary image, etc. belong to this group. These are relatively easy operations for analog implementations.

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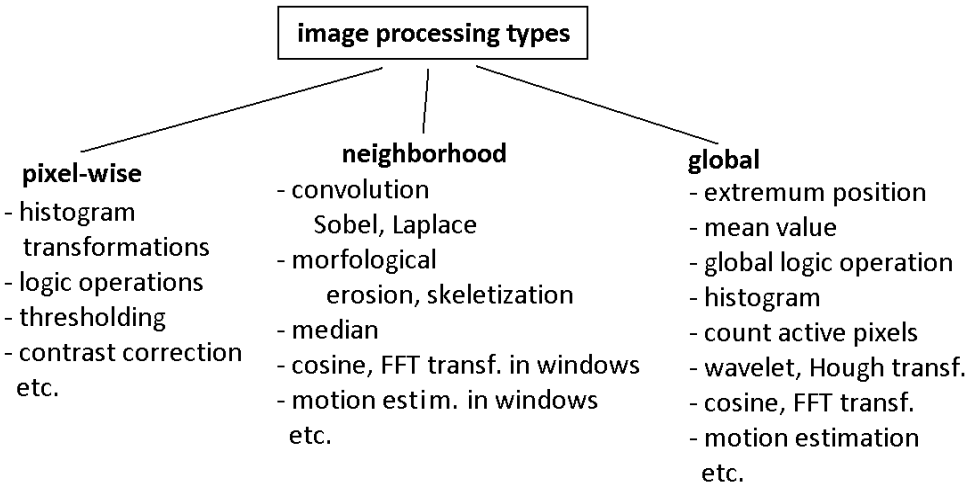

Fig. 2. Classification of operations carried out on images.

The filtering operations such as convolution and morphological transformations are based on information obtained from the processed pixel and from a number of its neighbors. Thus, in this case it is necessary to use a much more complex processor, which uses local connections between neighboring pixels.

Operations from the last group are typically used for feature extraction that relates to the entire image, for example: finding the location (coordinates) of the pixels with extreme values, a histogram calculation, determination of the number of active pixels on a binary image, calculation of Hough transform, etc. This type of operation requires a processor with high complexity that processes all the pixels in the image.

2.2. Architectures of integrated vision systems

There are three basic architectures of vision systems (Fig. 3): with a single separate processor, with an embedded array of processors (called processor-per-pixel architecture), and an intermediate solution with row processors (called row-fashion architecture). The selection of the vision system architecture is mainly dependent on the type of operations. In the case of analog implementations, the choice of architecture is also determined by other factors such as: sensitivity to components mismatch and technology variation, the required speed of image processing, or limitations on the supply power consumption.

2.2.1. Single processor architecture

The architecture with a separate processor has a very complex network of connections and a complicated addressing system, but it allows the use of a sophisticated processor, capable of executing complex and precise operations. The analog vision chips with a single processor architecture are frequently used to support MPEG and H.26x video compression, which are relatively complex algorithms. In [20-22] an implementation of a specialized single-chip digital camera is presented. In this case the processor cooperates with an RGB photosensitive matrix to generate the discrete cosine transform of an image. The micro camera was fabricated using a 0.8 μm CMOS. Another example of such a vision chip architecture is a motion estimation processor for low-power video coding. Realizations of a motion estimation processor in 0.13 μm, 1.2 μm and 0.8 μm CMOS technologies are presented in [23], [24] and [25]. In all these cases, the application of analog processors allows several times reduction of power consumption in comparison to digital solutions.

An interesting example of a vision chip with a single processor is presented in [26]. The chip contains a 128×109 photo-sensor matrix and an analog processor which can perform convolution filtering using a kernel with variable dimension from 2×2 to 128×109. That chip was fabricated in CMOS 0.5 µm technology, its maximal speed is 60 frames per second (fps) and power consumption is 60 mW.

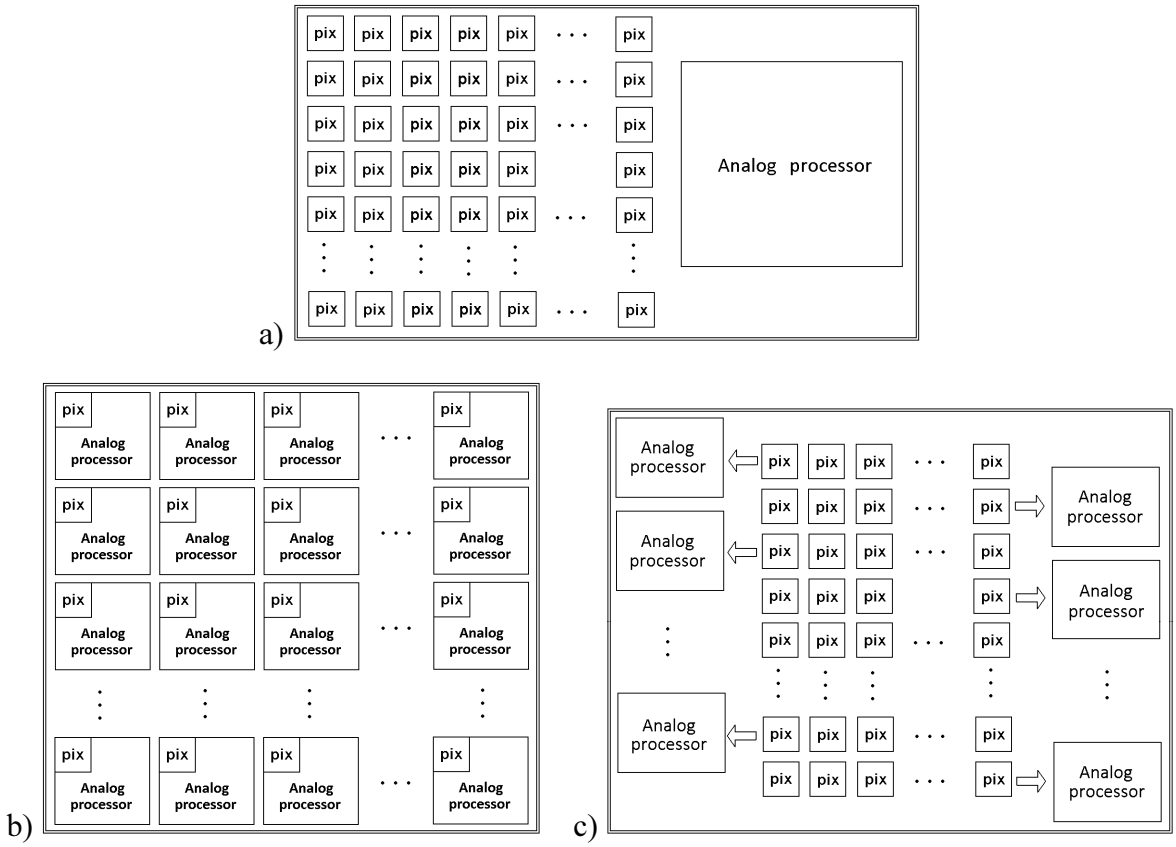

Fig. 3. Vision chip architectures: a) a single processor architecture, b) fully parallel with embedded array of processors, c) architecture with row processors.

2.2.2. Architecture with an embedded array of processors

In fully parallel vision systems, each photo-sensor has its own dedicated processor, as it is illustrated in Fig. 3b. This solution is ideal for implementing low-level convolution filtering, which is inherently parallel. In such a vision chip, at any given time exactly the same operation is done on each pixel. An additional advantage of this architecture is the ability to simultaneously process the signals coming from the neighboring pixels by a single dedicated processor. Therefore, there is no need for data transmission over longer distances and the number of data transfers from the pixels to the processors is reduced to a minimum. Consequently, the parallel architecture greatly increases the computational power, and allows image processing in real time with highly reduced power consumption. Despite the many advantages of such a solution, it has a significant limitation. In this kind of matrix only simple vision processors occupying a small area can be used, otherwise the size of the entire array, and consequently the cost of its production will become excessively large. Examples of implementations of such systems in 0.35 µm CMOS technology are presented in [6, 9, 15], and [27-31].

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2.2.3. Architecture with row processors

The architecture with row processors is a compromise between the previous architectures. An example of this kind of topology is shown in Fig. 3c. Due to the larger available space, more complex processors with a larger set of functions can be used, in comparison to the architecture with an array of processors. The application of the row processors also avoids the use of long-distance complicated interconnections, as it is the case with the single processor architecture. In this solution advanced techniques to reduce power consumption and noise correction can also be applied. Consequently, a higher image processing speed and lower power consumption are easily achieved. Vision chips of that kind are presented in [11, 32-34].

3. Switched current technique in image processing

In order to illustrate the specificity of analog processors design procedure, examples of SI filters design are presented in this section. The presented filters are based on the lossless multiport network configuration, which guarantees achieving filters with relatively low complexity and high signal processing efficiency. It is also shown that the design process of such filters can be significantly simplified by using an environment called gC-Studio. Two realizations of SI filters are presented. The first one includes an image detailed-emphasis filter, whereas the second includes a pair of filters which is applicable to: image compression, telecommunications systems and wireless communications.

3.1. Analog detailed-emphasis filter

It was shown in [35] that the problem of designing a two-dimensional analog filter given by the transfer function $H(z_1,z_2) = Y(z_1,z_2)/X(z_1,z_2)$ can be reduced to the problem of designing a one-dimensional lossless multiport network (LMN) with $x_i(s)$ excitation and $y_i(s)$ response signals. The indices "*i*" of $x_i(s)$ and $y_i(s)$ denote the inverse Z-transforms of signals $X(z_1,z_2)$ and $Y(z_1,z_2)$ with respect to variable z_1, where s is bilinearly transformed variable z_2. The general model of a lossless multiport element is presented in Fig. 4. The circuit is realized in SI technique and operates in the current mode. Hence, all signals: x_i, y_i and v_i mean the input or output currents of the corresponding blocks. The microcell with the label LMN is a counterpart circuit of a prototype lossless multiport network in which the symbols V_i denote voltages. The signals x_i, x_{i-1}, etc. are taken from the *i*-th, *i*-1-th etc. row of the image sensor matrix, while y_i signals are stored in the *i*-th row of the memory matrix.

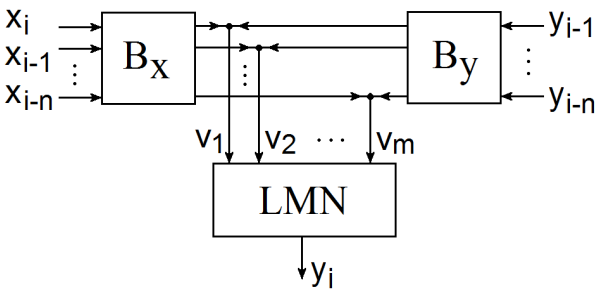

Fig. 4. General model of two-dimensional filtering reduced to the design of a lossless multiport network (LMN).

The complex CAD program tool called gC-Studio, discussed and described in [36], is used to design the lossless multiport networks. Its application and the effect of operation are

illustrated by the example of an image detailed-emphasis filter whose transfer function $H(z_1,z_2)$ is given by the coefficients of numerator and denominator matrices:

$$A = \begin{bmatrix} -0.0935 & 0.2810 & -0.0240 \\ 0.2971 & -0.1262 & -1.3423 \\ 0.0247 & -1.4017 & 4.2451 \end{bmatrix} \qquad B = \begin{bmatrix} 1.0000 & 0.2236 & 0.0715 \\ 0.2211 & 0.1545 & 0.1057 \\ 0.0917 & 0.1020 & 0.1563 \end{bmatrix} \tag{1}$$

corresponding to the nominator and denominator polynomials of the variables z_1, z_2 [35]. Fig. 5 illustrates the effect of using a filter simulated in a MATLAB environment. The original blurred image presented in Fig. 5A is processed with the use of a detailed-emphasis filter and presented in Fig. 5B.

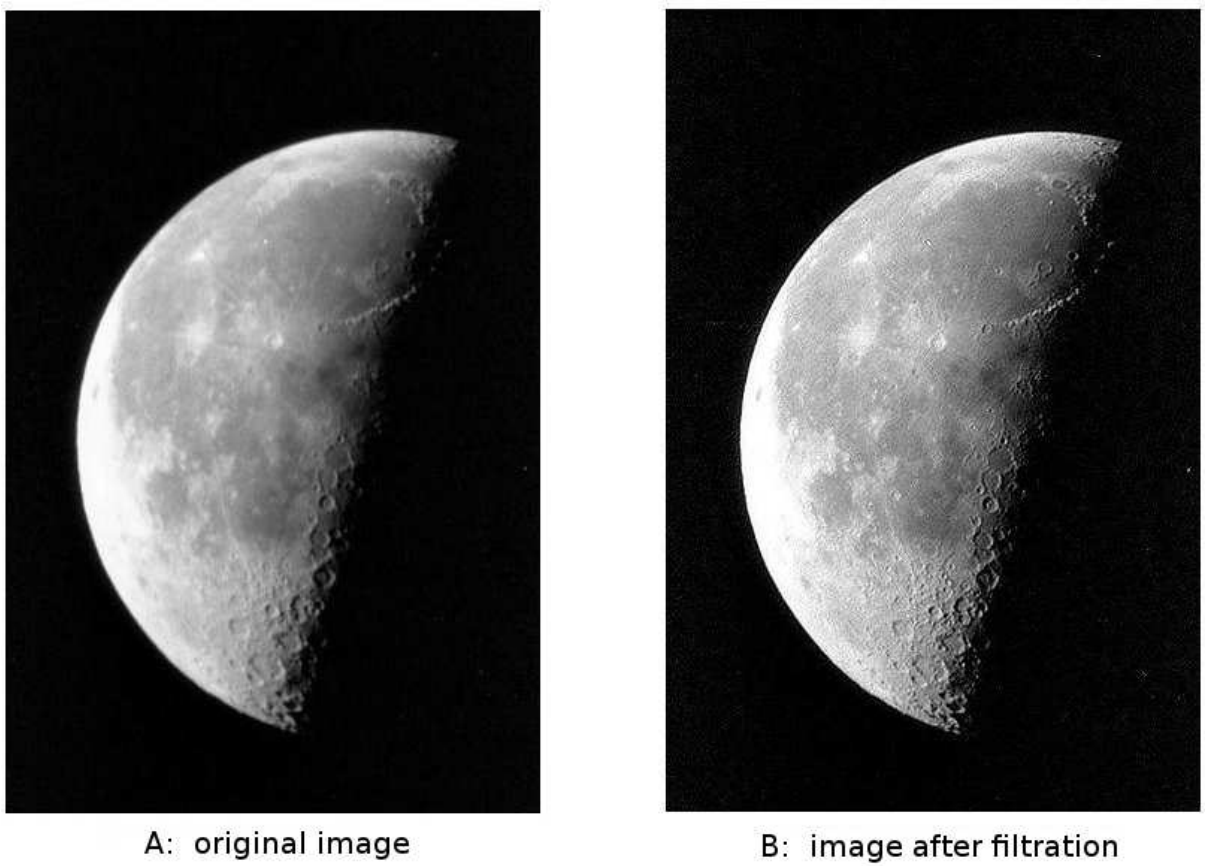

Fig. 5. The result of using a two-dimensional image detailed-emphasis filter. (A) – original image, (B) – image after filtering.

The gyrator-capacitor prototype circuit, designed using gC-Studio, and the counterpart LMN circuit are described using VHDL-AMS code. The reader can find in this description the details about the circuit elements: parameter values and connections of capacitors and gyrators. The elements of the matrices B_x and B_y denote the scaling factors of current mirrors which are used to realize the circuits B_x and B_y in Fig. 4. The matrices B_x and B_y are obtained from calculations, with the use of MATLAB, according to the formulas given in [35].

On the basis of a prototype lossless multiport network an SI counterpart circuit is obtained. This is a fully automated process with the use of a complex CAD tool called SI-Studio. The selected examples of the SI-Studio application are presented in [37]. The resulting SI filter consists of bilinear switched-current integrators [38] as well as

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parameterized current mirrors. The matrices B_x and B_y are also implemented using current mirrors.

3.2 Design process of SI filter pair

The CAD tools (gC-Studio, SI-studio) and the resulting SI prototype filters were verified using an ASIC integrated circuit implemented in TSMC (Taiwan Semiconductor Manufacturing Company) 180 nm CMOS technology, within the framework of project no. N N515 242937 of the National Science Center in Poland. The responses on low-pass and high-pass outputs of the 5-th order filter pair to a square wave excitation, observed on an oscilloscope are presented in Fig. 6. The current consumption was: 3.46 mA, 3.79 mA, and 5.34 mA, respectively for the circuit with long, intermediate, and short channel MOS transistors.

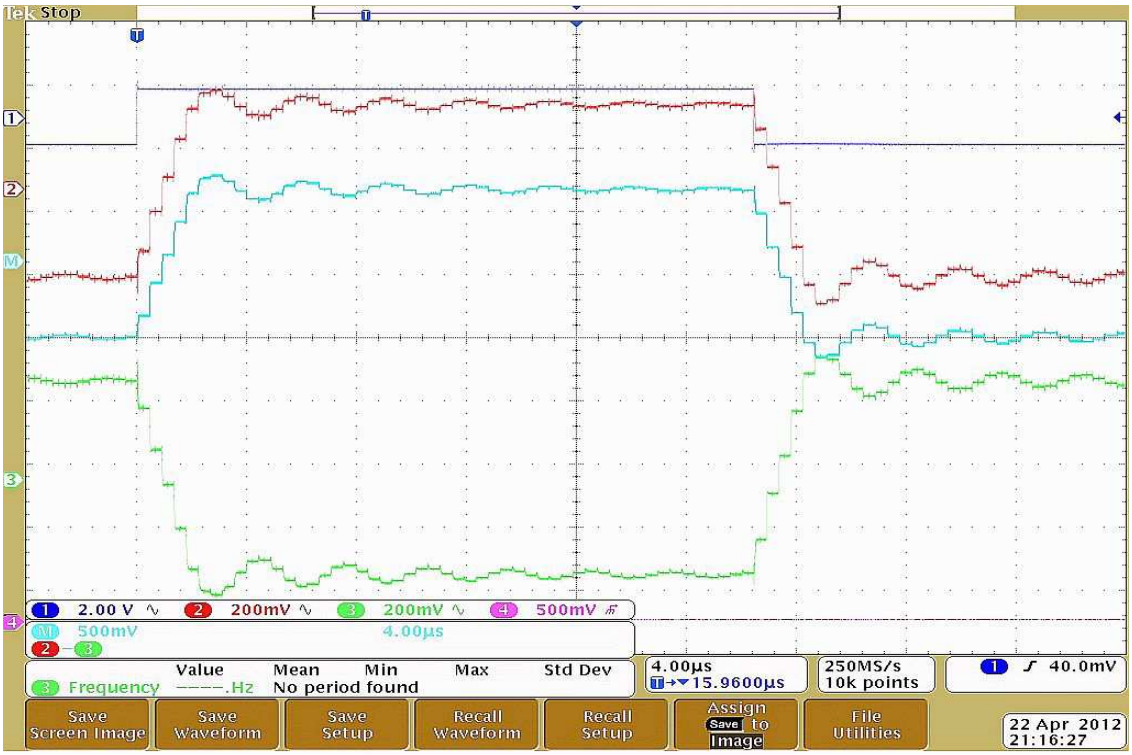

Fig. 6a. Results of measurement of an experimental filter pair fabricated in CMOS TSMC 180nm technology. Signals on low-pass outputs.

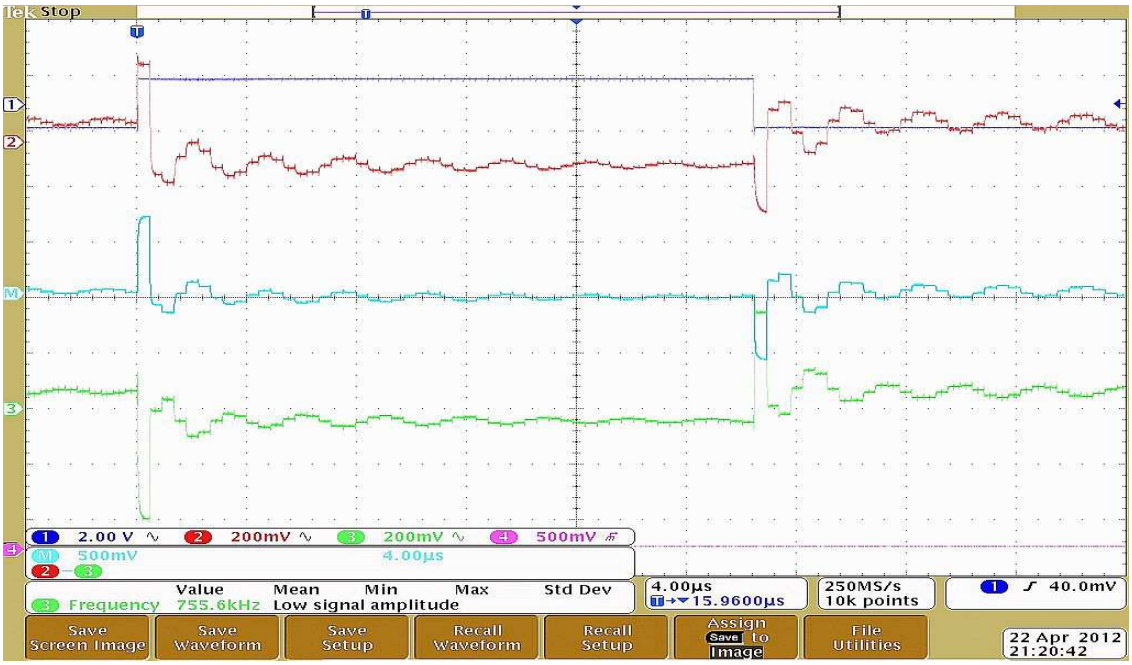

Fig. 6b. Results of measurement of an experimental filter pair fabricated in CMOS TSMC 180 nm technology. Signals on high-pass outputs.

In order to verify the correct operation of the filters, samples of the output signal were taken from the oscilloscope and next used to calculate the characteristics. In Fig. 7 the crosses represent the measured characteristics, whereas the solid lines represent the ideal ones. The achieved results confirm the proper operation of the prototype filters. This shows that in terms of image processing, it is possible to achieve satisfactory accuracy of signal processing.

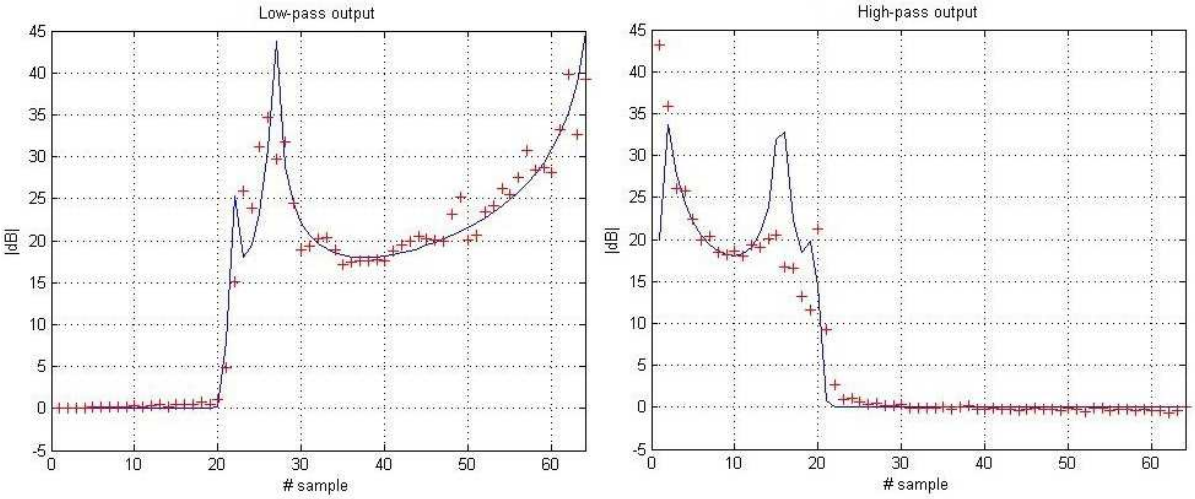

Fig. 7. Frequency characteristics of an experimental filter pair fabricated in 180nm CMOS TSMC technology for low-pass and high-pass outputs. (The Y axes denote attenuations of the filter pair and the sample #64 on the X axes denote the Nyquist frequency.)

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4. Conclusions

The paper characterizes the key features and methods of implementation of analog vision chips which are widely used in robotics and consumer equipment. Due to the rapid development of the smart devices, which mostly work based on the recording and analysis of images, the low-power, low-voltage, integrated vision sensors realized in cheap CMOS technologies become a great practical importance. With the possibility to design and implement a complete vision system on a single chip (SoC), the modern intelligent sensors can be implemented even in low-cost household appliances and toys, significantly improving their attractiveness and functionality. Due to the fact that the capacity of a standard CMOS technology becomes insufficient to realize high-resolution vision chips, the alternative solutions in the form of 3-dimensional (3D) chips [39] are under current research. Such solutions allow an independent implementation of image sensors with high-resolution, and the matrices of processors using different technologies best suited to the required functions.

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