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FAULTS CLASSIFICATION OF POWER ELECTRONIC CIRCUITS BASED ON A SUPPORT VECTOR DATA DESCRIPTION METHOD

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Abstract

Power electronic circuits (PECs) are prone to various failures, whose classification is of paramount importance. This paper presents a data-driven based fault diagnosis technique, which employs a support vector data description (SVDD) method to perform fault classification of PECs. In the presented method, fault signals (*e.g.* currents, voltages, *etc.*) are collected from accessible nodes of circuits, and then signal processing techniques (*e.g.* Fourier analysis, wavelet transform, *etc.*) are adopted to extract feature samples, which are subsequently used to perform offline machine learning. Finally, the SVDD classifier is used to implement fault classification task. However, in some cases, the conventional SVDD cannot achieve good classification performance, because this classifier may generate some so-called refusal areas (RAs), and in our design these RAs are resolved with the one-against-one support vector machine (SVM) classifier. The obtained experiment results from simulated and actual circuits demonstrate that the improved SVDD has a classification performance close to the conventional one-against-one SVM, and can be applied to fault classification of PECs in practice.

Keywords: power electronic circuit, fault classification, support vector data description, support vector machine.

1. Introduction

Power electronic circuits (PECs) can be easily found in industrial, military or civil applications, *e.g.* DC-AC inverters in motor drive circuits [1–3], rectifiers in AC-DC energy conversion systems [4], DC-DC converters in various structured switched-mode-powers (SMPs) [5–7], *etc*. In their applications, PECs are failure-prone, because they frequently experience current surges, continuous switching operations and high temperature stresses. Faulty PECs can result in serious aftermath, leading to money loss or even casualties. Hence, fault detection and localization of PECs are very important, and this can assure the reliability and availability of overall circuit systems. Also, fault diagnosis of PECs can supply necessary information for fault tolerant or even reconfiguration of the circuit systems [8].

Generally, fault diagnosis of a PEC can include two parts: fault detection and fault localization. A fault detection technique is used to detect whether the circuit is faulty, and fault localization can find the faulty components or sub-systems of the overall power electronic circuit system. In essence, fault diagnosis can be summarized to the problem of fault classification. The methods of diagnosing PECs can be grouped in two families. The first one is based on hardware design [6, 9], and this design will need the circuit mathematical model analysis. This method can be very fast, but seems to be inflexible when the circuit topology or the parameters of its component are changed. The other family is mainly based on the data and algorithm analysis, and this method does not need the explicit model of the circuit and is also called the data-driven method. The data-driven based fault diagnosis method is flexible in its algorithm design, which can be modified conveniently while the

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corresponding hardware remains unchanged. The data-driven based fault diagnosis method for PECs can be roughly divided into three steps. The first step is to collect original signals from circuits, and these original signals can be currents, voltages, or other information. Generally, these signals from a PEC contain noise disturbance, because of complicated working conditions. Therefore, in the second step, signal processing techniques are used to eliminate the noise disturbance, and then to extract the fault features. In the third step, algorithms are designed to implement the fault classification task. Design of the algorithms in this step is quite important, because it can directly affect the accuracy of fault classification.

In the last decades, some scientists have focused on designing fault diagnosis algorithms of PECs, and most of these algorithms are based on machine learning and pattern recognition techniques, which have been proven to be effective in the fault diagnosis domain of PECs [1]. Some scientists use the fuzzy inference technique, which seems to be effective in some industrial applications [10, 11]. In this method, a proper selection of memberships in the fuzzy algorithm is a difficult task. Neural classifiers are also applied to the fault diagnosis of PECs, because of its nonlinear mapping capability. For example, in [12], back-propagation neural network (BPNN) classifiers are used to diagnose switch faults of a three-phase inverter, and other applications of neural network classifiers to diagnose PECs can also be found in [13–15] and [16]. These applications demonstrate that the neural network classifiers are effective in fault classification of PECs.

The support vector machine (SVM) is another type of fault classifier, which has some good characteristics in pattern classification and regression in many applications [17]. The basic SVM implements binary classification and can be applied to fault detection of PECs. For example, in [18], the authors use the wavelet and waveform analysis to extract fault features from simulation data of an inverter, and finally the binary SVM is adopted to detect whether the inverter is faulty. A similar example can be found in [19], and in this case the Concordia transform is performed, based on three-phase currents of an inverter, to extract 2-dimensional fault features which are used to train the binary SVM. In some cases, the diagnosis technique needs to discern and locate the faulty components. Several multi-class SVM classifiers can be used for fault localization of PECs. One is called the one-against-rest SVM, and the other one – the one-against-one SVM. For example, in [4] and [20], the authors construct the one-against-rest SVM to perform fault classification of a three-phase rectifier. In [21], the one-against-rest SVM with Huffman tree structure is constructed to implement localization of a faulty switch in the simulated inverter.

This paper presents a fault classifier based on the support vector data description (SVDD), which, according to our knowledge, is seldom used in fault diagnosis of power electronic circuits. In this presentation, the SVDD is viewed as an alternative to the conventional multi-class SVM for fault diagnosis of PECs. In many cases, the SVDD cannot perform the fault diagnosis task well, because a feature sample probably falls into a so-called refusal area (RA), formed by two or more SVDD classifiers. Existing of RAs can reduce diagnosis accuracy. In our design, we consider to resolve the RAs by introducing the one-against-one SVM. This design can significantly improve the SVDD classifier performance. According to our investigations, this novel classifier is very fast, and it can achieve a comparable classification performance with the one-against-one SVM. Also, according to the results of experiments, the presented method outperforms the one-against-rest SVM and the designed three-layered BPNN classifier, in terms of training and classification performance.

The rest of the paper is arranged as follows. Section 2 introduces the basic principles of SVDD and RAs in detail. Also, in this section, the overall flowchart of the proposed approach is discussed. In Section 3, two PECs, including a simulated rectifier and an actual inverter, are described. In this section, open-faults for the switches are used, because these faults are general and typical in fault diagnosis applications of PECs. Feature extraction algorithms for

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experiments are also introduced in detail in this section. Results and their discussion are given at the end of this section. Finally, Section 4 presents the conclusions.

2. Method presentation

2.1. Basic theory for the SVDD

The presented fault diagnosis system for PECs employs the SVDD technique, which is regarded as the key pattern classification method in our design. The SVDD classifier is to map a set of samples, assumed to be $\{\boldsymbol{x}_i\}$ (i = 1, 2, ..., E, where E is the number of data samples), to a high-dimensional space, in which a spherically shaped boundary is formed to contain these data samples [22, 23]. The basic conception for the SVDD is shown in Fig. 1.

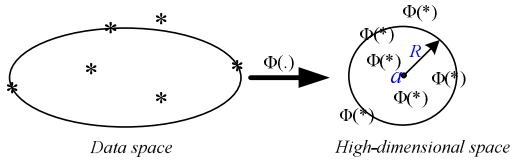

Fig. 1. The basic conception for the SVDD.

Assume the radius and center of this sphere to be R and $\boldsymbol{a}$, respectively; the following error function needs to be minimized:

$$F(R,\boldsymbol{a}) = R^2 + C\sum_{i=1}^{E}\xi_i \tag{1}$$

with the following constraint:

$$\left\|\Phi(\boldsymbol{x}_i) - \boldsymbol{a}\right\|^2 \le R^2 + \xi_i\,,\ \ \xi_i \ge 0, \forall i\,, \tag{2}$$

where $\Phi(\boldsymbol{x}_j)$ is the mapping function, which can map the data samples to a high-dimensional space; ξ_i are the slack variables allowing some samples to be outside of the sphere; C is the penalty parameter to control the balance of sphere volume and classification errors.

By introducing Lagrange multipliers and partial derivatives, we can solve this quadratic optimization problem and obtain the sphere center [22]:

$$\boldsymbol{a} = \sum_{j=1}^{S}\alpha_j\Phi(\boldsymbol{x}_j)\,, \tag{3}$$

where S is the number of support vectors; $0 < \alpha_j < C$ is the Lagrange multiplier of the j-th sample $\Phi(\boldsymbol{x}_j)$.

Assume $\boldsymbol{x}_m, \boldsymbol{x}_n$ to be the m-th and nth support vector (m, n = 1, 2, ... , S), respectively. By using the kernel function $K(\boldsymbol{x}_m,\boldsymbol{x}_n) = <\Phi(\boldsymbol{x}_m),\Phi(\boldsymbol{x}_n)>$, where $<,>$ is the inner product, R can be computed with any support vector (*e.g.*, $\Phi(\boldsymbol{x}_m)$) on the sphere:

$$\begin{aligned} R &= \sqrt{[\Phi(\boldsymbol{x}_m) - \boldsymbol{a}]^2} \\ &= \sqrt{[K(\boldsymbol{x}_m,\boldsymbol{x}_m) - 2\sum_{j=1}^{S}\alpha_j K(\boldsymbol{x}_j,\boldsymbol{x}_m) + \sum_{j=1}^{S}\sum_{t=1}^{S}\alpha_j\alpha_t K(\boldsymbol{x}_j,\boldsymbol{x}_t)]}. \end{aligned} \tag{4}$$

The SVDD can be used to classify faults of PECs. For N faults, N SVDD classifiers need to be established. The lth fault class (l = 1, 2, ..., N) corresponds to the lth SVDD classifier. To test an unknown sample $\boldsymbol{z}$, whose form is $\Phi(z)$ in the high-dimensional space, the

distances to each centre of the SVDD classifiers have to be computed. Assume R_l, $\boldsymbol{a}_l$ to be the radius and centre of the lth SVDD, respectively. Then, the distance between $\Phi(z)$ and $\boldsymbol{a}_l$ becomes:

$$dist_l = \sqrt{(\Phi(z) - \boldsymbol{a}_l)^2}, l = 1, 2, ..., N . \tag{5}$$

Generally, the following two cases are considered for the lth SVDD classifier:

Case I : If $dist_l \le R_l$, the sample $\Phi(z)$ falls into or on the sphere. In this case, the sample is considered to belong to the lth fault class.

Case II: Otherwise, the sample $\Phi(z)$ falls outside of the sphere. This case shows this sample does not belong to the lth class. In other words, it belongs to another class, so it can be rejected by the diagnosis system.

2.2. RA of the SVDD classifiers

In applications of fault classification using SVDD classifiers, a sample to be tested will probably fall into a so called refusal area (RA), as shown in Fig. 2.

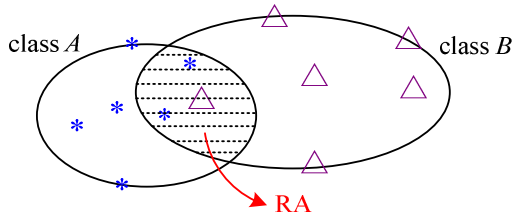

Fig. 2. One RA formed by two classes.

RA is a public area, which can be formed by two or more SVDD classifiers. In Fig. 2, a RA is generated by two SVDD classifiers, class A (indicated with "*") and class B (indicated with "△"). In this paper, for simplicity, we discuss the RA in the original data space, not in the high-dimensional space. If a sample (assumed to be a "△", shown in Fig. 2) falls into the RA, this means the sample can either be assigned to class A or be assigned to class B. Sometimes, the sample to be tested falls outside of all the SVDD classifiers. In such a case, the sample is considered to fall into an unknown area, which is called the special RA in this paper.

The existence of RAs can degrade the classification performance of conventional SVDD, resulting in its application to the PEC fault diagnosis being impractical. Hence, we consider performing classification in this area by using an SVM classifier. Similarly to the SVDD classifier, the SVM implements the classification task via the kernel function in the high-dimensional space, in which a linear boundary can be formed [24, 25]. A basic binary SVM (BSVM) classifier can perform binary classification, and for a multi-class problem an ensemble of BSVM classifiers can be employed [26]. SVM classifiers, including the one-against-rest and one-against-one structures [27–29], have been applied to electronic circuit fault diagnosis. For N faults, the one-against-rest SVM needs N BSVM classifiers, whereas for the one-against-one SVM $N(N\text{-}1)/2$ BSVM classifiers need to be considered. In this paper, the one-against-one SVM is adopted as the auxiliary classifier to classify samples falling into the RA formed by SVDD classifiers, because this classifier has a good performance in electronic circuit fault diagnosis [30].

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2.3. SVDD classifier improved by the SVM

In testing an unknown sample z, the SVDD method is the master classifier and the one-against-one SVM can be viewed as an auxiliary classifier for improvement. For N fault classes, the decision steps for the improved SVDD classifier are showcased in Fig. 3. Initially, distances between sample z and N SVDD classifiers need to be calculated, and sample z should be assigned to the class, which is corresponding to the smallest distance. When z falls into the RA, the one-against-one SVM classifier is activated.

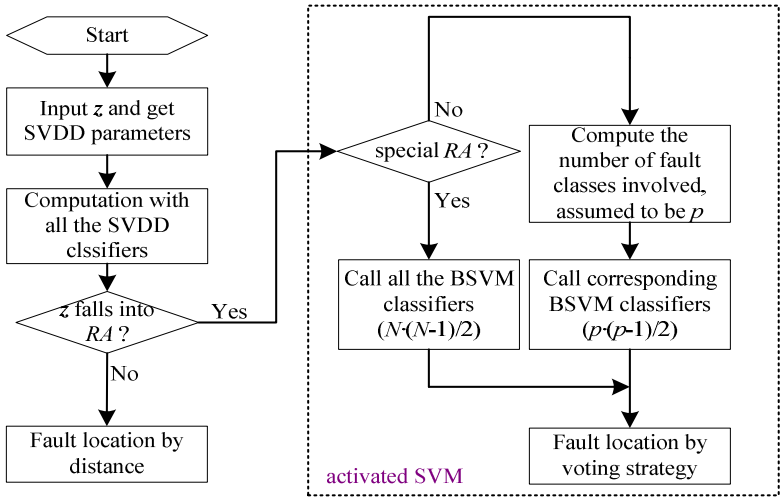

Fig. 3. The presented SVDD method improved by the SVM classifier.

Figure 3 shows the process of fault class assignment using the one-against-one SVM, and this process is enclosed within the dotted-line area. In this case, not all the BSVM classifiers are required to participate in the computation. Only those BSVM classifiers, whose corresponding fault classes form the RA, are necessary in this calculation. Assume the number of involved fault classes to be p ($p \geqslant 2$), then the number of expected BSVM classifiers should be $p(p-1)/2$. The final fault class assignment is also implemented according to the voting strategy among these p classes. Once z falls into the special RA, the complete calculation of the one-against-one SVM is needed. In this case, the number of BSVM classifiers can reach $N(N-1)/2$.

With an increase of N, the computation cost for the one-against-one SVM will increase drastically. By contrast, an increase of the computation cost for the SVDD approach is not significant. By using this new classifier, our diagnosis system can achieve a good classification performance, which can be close to that of the one-against-one SVM. Meanwhile, the computation cost can be apparently reduced as well. Also, compared with some conventional fault classifiers (such as the one-against-rest SVM, neural classifier), the presented method has a very high training speed. The following experiments vindicate effectiveness of this method.

3. The experiments

3.1. The first simulated circuit

3.1.1. Simulation setup

The first power electronic circuit is a three-phase full-bridge rectifier with six controlled thyristors, shown in Fig. 4. This circuit is modeled and simulated with the Matlab – Simulink software. In this simulation, R_{load} is set to be 100 Ω; L_{load} is 1.5 H; the nominal phase frequency and RMS (Root-Mean-Square) voltage for the input source (u_U, u_V and u_W) are 50 Hz and 220 V, respectively; the firing angles for the thyristors range from 0° to 90° with which this circuit can act as a rectifier. The terminal voltage u_d is selected as the accessible signal, which is sampled 50 times and each time the firing angle is varied evenly. In the simulation setup, the sampling frequency for the data is set to be 20 KHz and for each sample 1200 data dots are sampled. Hence, each sample generation consumes 60 milliseconds. The sampled 1200 dots contain several waveform periods and this can help to extract features in the frequency domain.

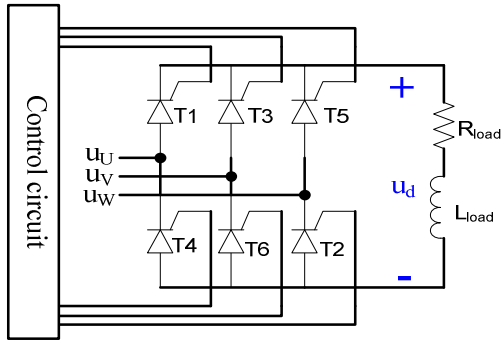

Fig. 4. The simulated three-phase full-bridge rectifier.

In this circuit, two cases are considered. In the first case, only five fault classes are used. In the other case, 22 classes are considered. The two cases are mainly used to investigate the performance of classifiers under different numbers of faults. Open-circuit faults for the thyristors are investigated. Fault sets for the first and second case are listed in Table 1 and Table 2, respectively. {Tf, Tg} (f, g = 1, 2, 3, 4, 5, 6, and $f \neq g$) means two thyristors Tf and Tg are faulty simultaneously. In this research, f0, indicating a healthy circuit, is regarded as a special fault class.

Table 1. Fault classes for the first circuit (1st case).

FAULT CODE	DESCRIPTION
f0	The circuit is healthy
f1	T1 or T2 or T3 or T4 or T5 or T6 is faulty
f2	{T1, T4} or {T3, T6} or {T2, T5} are faulty
f3	{T1, T3} or {T1, T5} or {T3, T5} or {T2, T4} or {T2, T6} or {T4, T6} are faulty
f4	{T1, T2} or {T2, T3} or {T3, T4} or {T4, T5} or {T5, T6} or {T6, T1} are faulty

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Table 2. Fault classes for the first circuit (2nd case).

FAULT CODE	DESCRIPTION	FAULT CODE	DESCRIPTION
f0	The circuit is healthy	f11	{T1, T5} are faulty
f1	T1 is faulty	f12	{T2, T4} are faulty
f2	T2 is faulty	f13	{T2, T6} are faulty
f3	T3 is faulty	f14	{T3, T5} are faulty
f4	T4 is faulty	f15	{T4, T6} are faulty
f5	T5 is faulty	f16	{T1, T2} are faulty
f6	T6 is faulty	f17	{T2, T3} are faulty
f7	{T1, T4} are faulty	f18	{T3, T4} are faulty
f8	{T3, T6} are faulty	f19	{T4, T5} are faulty
f9	{T2, T5} are faulty	f20	{T5, T6} are faulty
f10	{T1, T3} are faulty	f21	{T6, T1} are faulty

3.1.2. Feature extraction for the rectifier

The waveforms of u_d can be different even for the same fault class, because the firing angle can be various. Hence, the time domain analysis for the u_d is difficult. In this paper, we analyze the waveforms of u_d in the frequency domain, because different faults can result in fluctuation of different harmonic components. The Fast Fourier Transform (FFT) analysis is applied to u_d waveforms. For the FFT analysis, assume H_q and A_h to be the spectrum amplitude of the q-th harmonic component (q = 0, 1, 2, 3 …) and the phase angle of hth harmonic component (h = 1, 2, 3 …), respectively. Here, H_0 refers to the DC component of the signal, H_1 is the fundamental harmonic component, H_2 is the second harmonic component, and so on. The FFT analysis can generate numerous features. However, not all features can contribute to the final fault classification. Hence, the feature selection is an important task. In this investigation, we attempt to use a combination of some features (from H_q and A_h, q = 0, 1, 2, 3 …, h = 1, 2, 3 …), and then use the one-against-one SVM classifier to testify effectiveness of this combination. Once a good testing accuracy of this SVM classifier is achieved for the testing data, this combination is considered to be effective. In fact, this technique belongs to a wrapper based feature selection method [31].

In our feature selection experiment, first a combination of spectrum amplitude features is considered, because these features are frequently used in fault diagnosis applications. The combination set of features is initialized with [H_0, H_1], and then the SVM classifier is used to testify effectiveness of this combination. If the classification accuracy of the SVM is not ideal, the combination set of features is changed by adding another feature to it, and the testing procedure is restarted, until a good classifier performance is achieved. In order to reduce the feature selection time, in our experiment q and h are limited to not exceed 6. After the feature selection, a 3-dimensional feature [H_0, H_1, H_2] is found to be enough for distinguishing 5 fault classes. Classification of 22 fault classes will need a 13-dimensional feature [cosA_1, cosA_2, cosA_3, cosA_4, cosA_5, cosA_6, H_0, H_1, H_2, H_3, H_4, H_5, H_6], with which a good classification performance of the classifiers can be achieved.

3.1.3. Classifier training and results

Five pattern classifiers are used in this paper for the performance comparison. The first one is the one-against-rest SVM, which adopts the Winner-Takes-All (WTA) strategy [32]. The second is the one-against-one SVM, which employs the voting strategy in the decision process. The conventional SVDD is the third classifier. Our presented improved SVDD (indicated with "iSVDD") is the fourth classifier. A three-layered BPNN is the final designed classifier, because it is widely used in the domain of circuit fault diagnosis.

In the first case for diagnosing 5 classes, five SVDD classifiers are established. Also, five and ten BSVM classifiers for the one-against-rest and one-against-one SVM are constructed, respectively. Thirteen samples for each fault class are selected as the training data, and the other thirty-seven samples are for the purpose of testing. All the samples are normalized to have zero-mean-values and unity variance. In the SVM and SVDD training process, the penalty parameter C is set to be 100, and the kernel function is selected as the radial-basis-function (RBF) $K(x,y)=e^{-\|x-y\|^2/\sigma^2}$, where σ is the kernel function parameter. The kernel RBF is a commonly used function and adoption of this function leads to good classification results. Different kernel parameters will result in different results, and in this experiment good results can be achieved when σ is set to 1. In our experiment, we consider using the standard SVM because this classifier has a good generalization performance. In training the neural classifier, the Levenberg-Marquardt algorithm is used. The number of hidden layer neurons is 4, and the activation function from the input layer to the hidden layer is *tansig*. The BPNN training is implemented with the *newff* function in the Matlab 2010 software, and the NN uses *sim* function for testing. Different trainings for the BPNN will probably result in different performances. In our example, the BPNN is trained for three times, and the best performance is selected as the final result of neural classifier. The final and detailed classification results for five classifiers are listed in Table 3.

Table 3. The classification results of 5 faults for the rectifier (1st case).

CLASSIFIER	ACCURACY (×100%)	TESTING TIME (S)	TRAINING TIME (S)	NUMBER OF SVs
One-against-rest SVM	1.000	0.722	0.414	91
One-against-one SVM	1.000	1.440	0.354	81
BPNN	1.000	3.933	0.334	–
SVDD	0.861	0.597	0.073	22
iSVDD	1.000	0.825	0.073	＞22

In this table, the testing accuracy, the time for testing and training, as well as the number of consumed support vectors (SVs) in performing the calculation of SVM and SVDD, are shown. In Table 3, the conventional SVDD method can classify 86.1% of the testing samples. The other two SVM classifiers demonstrate 100% classification accuracy for the testing samples. The iSVDD can classify all the samples rightly, illustrating an ideal classification performance after improvement. In terms of testing time, the one-against-one SVM consumes 1.44 seconds to perform the classification task, whereas the iSVDD consumes less time (0.825 seconds).

In diagnosing 22 fault classes, the number of training samples for each class is increased to 20, with which a very high classification accuracy can be achieved. In this experiment, the kernel parameter σ is equal to 2 for several support vector classifiers. The number of BPNN hidden layer neurons is 13, and in this example the BPNN cannot converge to the goal error. Hence, the result for the BPNN is excluded from this example. The final and detailed results of diagnosing the rectifier in the second case are listed in Table 4.

Table 4. The classification results of 22 faults for the rectifier (2nd case).

CLASSIFIER	ACCURACY (×100%)	TESTING TIME (S)	TRAINING TIME (S)	NUMBER OF SVs
One-against-rest SVM	0.991	22.159	3.173	5913
One-against-one SVM	0.991	132.050	6.145	9385
SVDD	0.538	10.711	0.317	358
iSVDD	0.991	75.982	0.323	＞358

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In this case, the SVDD can classify only 53.8% samples in the testing phase, and the other three classifiers can achieve a very high classification accuracy of 99%. The one-against-one SVM classifier needs about 132 seconds to classify 22 fault classes (20 samples for each class) and the iSVDD also consumes a lot of time (about 76 seconds) to perform classification, because, in this case, the classifier improvement needs to calculate many extra BSVM classifiers.

Also in this case, we investigate the impact of kernel RGF parameter σ on the classification performance of support vector classifiers. With this, the comparison of classification accuracy for 4 classifiers in testing is presented in Fig. 5. In this experiment, σ is set to be 1, 2, 4, 8, 16, 32 and 64 in order. In this figure, the logarithmic coordinate ($\log_{10}^{\sigma}$) is used for convenience of observation.

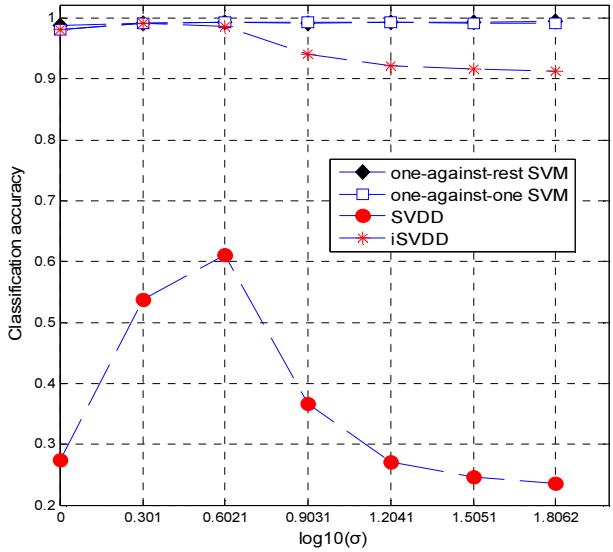

Fig. 5. The comparison of classification accuracy for 4 classifiers regarding σ (the rectifier).

From Fig. 5, we can see that the SVDD classifier displays a poor performance with various kernel parameters. Although the iSVDD performance curve has a slight fluctuation in this figure when σ is larger than 4, its overall classification accuracy is still above 90%. The classification accuracy for two SVM classifiers is almost perfect.

3.2. The second actual circuit

3.2.1. Experiment platform description

The second PEC, shown in Fig. 6, is an actual three-phase inverter in a motor-drive.
The AC motor used in our experiment is a three-phase (phase A, phase B, and phase C), 5-pair poles, 50 W brushless DC motor, whose shaft is coupled to an electric fan as the load with rated speed of ~ 800 rpm. The power switches used in the drive circuit are MOSFETs, driven with the square wave pulse width modulation (PWM), and the input DC voltage Vdc is +48 V. For simplicity, we consider a single switch fault for the drive circuit. Altogether 7 patterns need to be classified, and here the healthy condition of the circuit is regarded as a special fault pattern. In this example, the fault code for a faulty switch T*i* is f*i* (*i* = 0, 1, 2, 3, 4, 5 and 6), where f0 denotes a healthy circuit.

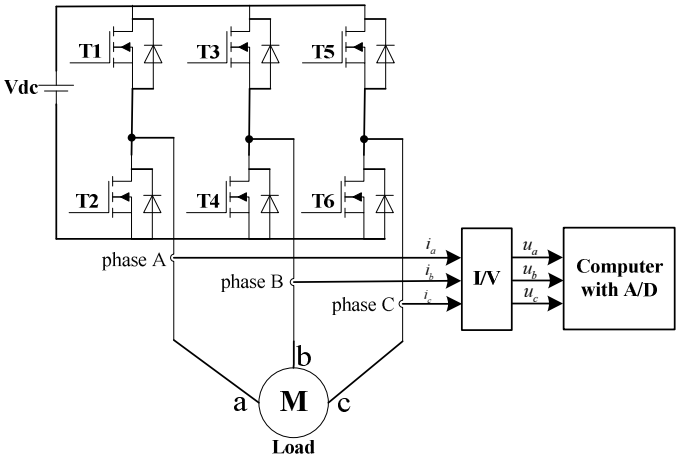

Fig. 6. The inverter under investigation.

Three-phase currents (i_a, i_b, i_c) need to be collected synchronously. We have designed an I/V interface circuit to change the currents into voltages, which are sampled by a 12-bit A/D unit and sent to the computer. The basic platform is shown in Fig. 7.

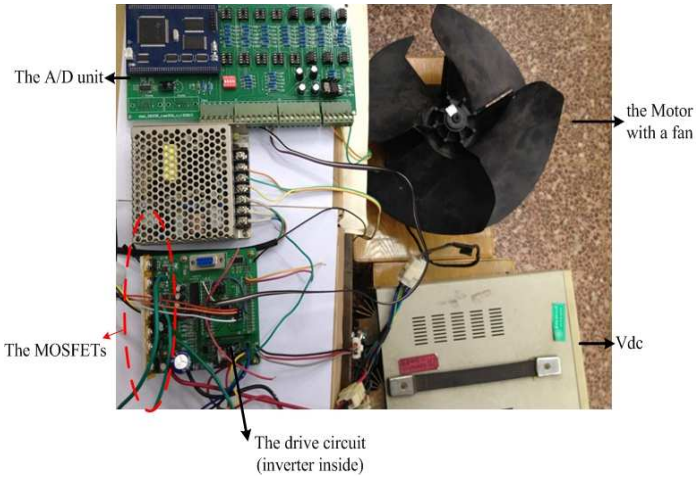

Fig. 7. The experiment platform for the second PEC.

3.2.2. Feature extraction for the inverter

By changing the speed of load from 700 rpm to 900 rpm, we collect the three-phase currents. For each fault class, forty actual data samples are collected. For each data sample, the A/D unit consumes about 8.32 milliseconds to implement the data acquisition operation.

In order to reduce the noise effect, the wavelet transform (WT) is performed to process three-phase currents. The wavelet mother function is hard to select, and we find a good one through the experiment results. Finally, *Haar* wavelet is adopted as the mother function to decompose the current signals into coarse coefficients (i_a^w, i_b^w, i_c^w) and detailed coefficients at

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level 3. The coarse coefficients can describe the waveform outline, which is enough to distinguish different open-switch faults, and thus are considered to be informative and useful.

The detailed coefficients are not used in our design. In order to reduce the impact of load on our design, the wavelet coefficients are furthermore normalized:

$$\begin{cases} \hat{i}_a = i_a^w / \max(\text{abs}(i_a^w)) \\ \hat{i}_b = i_b^w / \max(\text{abs}(i_b^w)) \\ \hat{i}_c = i_c^w / \max(\text{abs}(i_c^w)) \end{cases}, \tag{6}$$

where abs(.) and max(.) are functions to obtain, respectively, the absolute and maximum values from the corresponding wavelet coefficients.

For an AC motor system with symmetrical structure, the Concordia transform of phase current is used to calculate the current trajectory ($\hat{i}_\alpha, \hat{i}_\beta$) in the $\alpha\beta$-frame:

$$\begin{cases} \hat{i}_\alpha = (2\hat{i}_a - \hat{i}_b - \hat{i}_c)/\sqrt{6} \\ \hat{i}_\beta = (\hat{i}_b - \hat{i}_c)/\sqrt{2} \end{cases}. \tag{7}$$

Moreover, a two-dimensional feature [C_α, C_β] is extracted from the trajectory:

$$\begin{cases} C_\alpha = \dfrac{1}{M}\displaystyle\sum_{k=1}^{M} \hat{i}_\alpha(k)/r \\ C_\beta = \dfrac{1}{M}\displaystyle\sum_{k=1}^{M} \hat{i}_\beta(k)/r \end{cases}, \tag{8}$$

where $r = \dfrac{1}{M}\displaystyle\sum_{k=1}^{M}\sqrt{(\hat{i}_\alpha(k) - \dfrac{1}{M}\sum_{k=1}^{M}\hat{i}_\alpha(k))^2 + (\hat{i}_\beta(k) - \dfrac{1}{M}\sum_{k=1}^{M}\hat{i}_\beta(k))^2}$ is regarded as the average radius size from the centroid to the trajectory boundary; M is the number of data dots forming the trajectory after WT (in this investigation M = 724), with which a complete trajectory can be formed; k is the index for the sampled data (k = 1, 2, 3, …, M).

Two features can roughly describe the centroid of trajectory with respect to its radius.

3.2.3. The results

The feature extraction technique is quite effective. Fig. 8 shows the impact of WT on the waveforms of currents during open fault at T1. In this figure, (a1), (a2) and (a3) represent three-phase currents, respectively, and (b1), (b2) and (b3) are their corresponding results after WT and the normalization process. It is apparent that the current waveforms become clear after the wavelet signal processing, and the signal amplitudes are also normalized to the range of [–1, +1], which can be observed easily from (b1), (b2) and (b3).

In this example, each fault class has 14 samples for training and the remaining 26 samples for testing. Seven SVDD classifiers are established for machine learning. Also, seven and twenty-one BSVM classifiers are generated for the one-against-rest SVM and the one-against-one SVM, respectively. The penalty parameter C is set to be 100 and σ equals 2. With these parameters, several support vector classifiers can achieve a good classification performance. The hidden layer of BPNN contains 6 neurons, and the activation function from the input layer to the hidden layer is selected as *logsig*, with which good results can be obtained. Table 5 gives the final results.

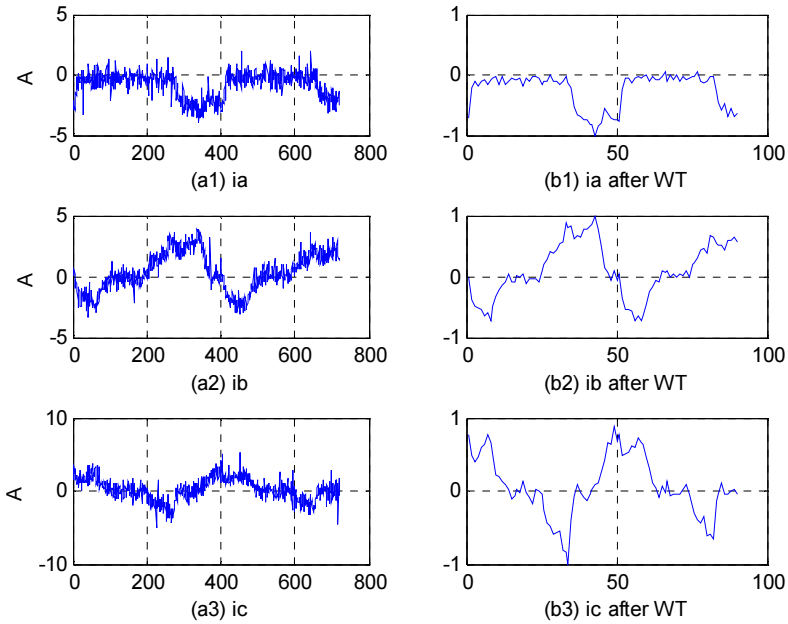

Fig. 8. Three-phase current waveforms of inverter before and after WT during open fault at T1.

Table 5. The classification results of 7 faults for the inverter.

CLASSIFIER	ACCURACY (×100%)	TESTING TIME (S)	TRAINING TIME (S)	NUMBER OF SVs
One-against-rest SVM	0.940	1.094	1.038	94
One-against-one SVM	0.967	3.247	0.570	70
BPNN	0.918	4.460	0.812	–
SVDD	0.786	0.947	0.094	16
iSVDD	0.956	1.273	0.094	＞16

In this experiment, with no more than 1 second in testing, the iSVDD can achieve 95.6% accuracy, which is close to the one-against-one SVM, and we can also observe that the SVDD training needs very little time. The neural classifier can achieve 91.8% accuracy, but it needs 0.812 and 4.46 seconds to perform the training and testing tasks, respectively.

In this example, we still investigate the impact of kernel parameter σ on the classification performance of four classifiers. The curves of classification accuracy for the classifiers, corresponding to the values of σ, are shown in Fig. 9.

In Fig. 9, it is clear that the iSVDD has a performance very close to the one-against-one SVM, whereas, in this example, the one-against-rest SVM shows a significant performance fluctuation when the value of σ is increased. The one-against-one SVM still demonstrates a good performance in diagnosing this PEC and this is the main reason of selecting it as the auxiliary classifier of conventional SVDD.

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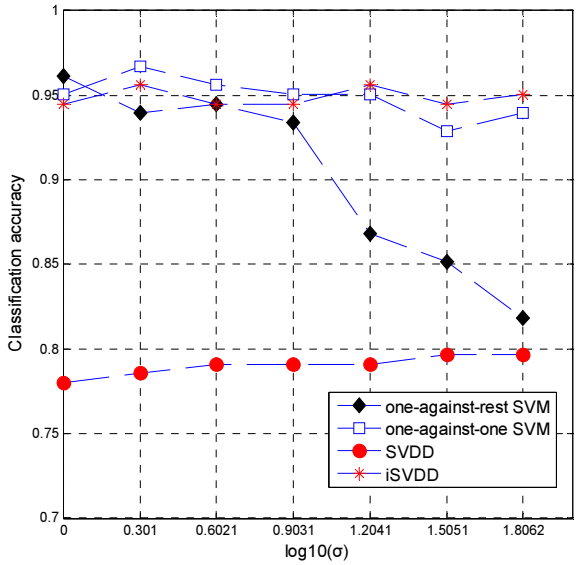

Fig. 9. The comparison of classification accuracy for 4 classifiers regarding σ (the inverter).

3.3. Analysis of results

Two experiments indicate that the SVM classifiers, together with the BPNN classifier, can be applied to fault classification of power electronic circuits. Among these classifiers, the one-against-one SVM has an excellent classification performance even if the kernel parameter is varied. However, the one-against-one SVM consumes a lot of time to implement fault classification, because this classifier needs to compute many BSVM classifiers, whose number will increase drastically with the increasing number of fault classes.

The experiments also indicate that the SVDD method can be applied to fault classification of power electronic circuits. However, this classifier needs to be improved, because samples can fall into the RA. This phenomenon can be observed directly from the 2-dimensional data distribution space in diagnosing the actual inverter. Fig. 10 displays SVDD boundaries of the fault samples of inverter in the original data space. In this Figure, seven enclosed boundaries indicating corresponding faults (f0, f1, …, f5 and f6) are plotted and these RAs can be easily observed directly. For example, the RA formed by class f4 and f5 is clear in this 2-dimensional picture. In addition, the area outside all the boundaries is regarded as the special RA.

The RAs must be resolved for improving performance of the SVDD method. The results for two circuits indicate that the presented iSVDD can achieve a significant performance improvement over the SVDD. However, this improvement needs to calculate extra BSVM classifiers. Hence, compared to the conventional SVDD method, the time consumption for the iSVDD is increased. Despite that, the iSVDD consumes less time in testing than the one-against-one SVM does. Also, from the results we can see that both testing and training for the conventional SVDD classifier is very fast. This is another reason why we adopt this classifier as the fault classification tool of PECs.

The BPNN is also a good classifier in fault classification. It demonstrates a good performance in diagnosing 5 faults in the rectifier and 7 faults in the inverter. However, in our investigations this classifier cannot converge in training 22 fault classes for the first PEC. In order to solve this problem, some additional methods, *e.g.* a classifier group technique can be

used [12, 33]. However, to the way of improving the BPNN classifier will not be discussed in this paper.

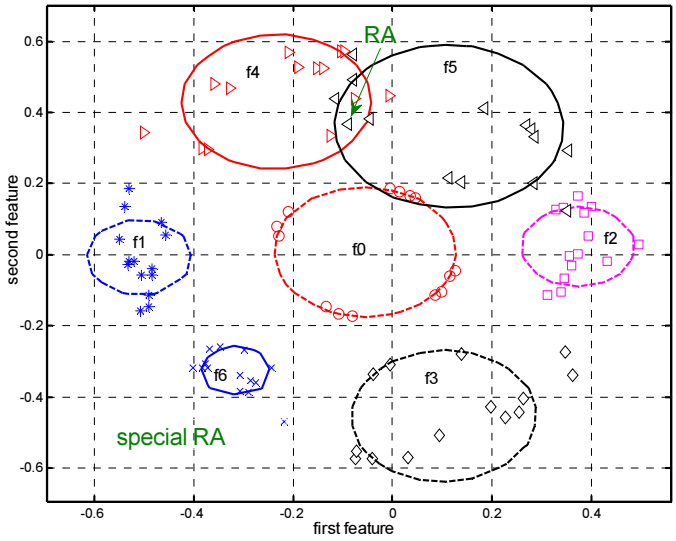

Fig. 10. SVDD boundaries in the original data space for the inverter.

4. Conclusions

This paper presents a method of PEC fault classification based on the iSVDD classifier. The conventional SVDD has a very high training and testing speed. But, in many cases, this classifier has a poor classification performance and, therefore, needs to be improved. In our research, the one-against-one SVM is adopted to implement the improvement task. After the improvement, the iSVDD is found to have its performance very close to the one-against-one SVM. Moreover, it needs much less time in testing. This indicates that the presented iSVDD can be considered as an alternative to the one-against-one SVM. In comparison with the conventional SVDD, the presented method can achieve a significant performance improvement, which is at the cost of some extra calculations of BSVM. Also, considering the variation of kernel parameter, the presented method demonstrates a good and relatively stable classification performance. In our investigations, the BPNN classifier is also suited for the fault diagnosis task, but this classifier shows an unreliable performance because different trainings probably lead to different results [28, 34]. In the first example, the BPNN cannot even converge in training 22 fault classes. In our research, among three trainings, the best performance of the BPNN is selected for the purpose of comparison. Despite this, the designed neural classifier seems to be inferior to the presented method.

In our research, the SVDD classifier is improved by the one-against-one SVM and this improvement is proved to be effective. Other methods can also be considered to improve the conventional SVDD classifier, and these methods will be envisaged in our future work.

On the other hand, the illustrated fault class setup for the power electronic circuit seems to be direct and simple, and only the open fault for the power switch is considered. In fact, some more complicated fault classes exist in an electronic circuit. For instance, in [35], the beta forward factor of a transistor is considered as a potentially faulty parameter and this parameter is considered to be important in predicting a component fault. Our next work will also consider a more complex and practical fault class setup.

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